1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,MBP15

04/24/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	N/A	N/A
2	2	System Block Diagram	(T9_MLB)	08/23/2006
3	3	Power Block Diagram	(T9_MLB)	08/23/2006
4	4	Power Block Diagram	N/A	N/A
5	5	BOM Configuration	N/A	N/A
6	6	Revision History	N/A	N/A
7	7	Functional / ICT Test	(MASTER)	(MASTER)
8	8	Power Aliases	(MASTER)	(MASTER)
9	9	Signal Aliases	(T9_MLB)	08/23/2006
10	10	CPU FSB	T9_NOME	03/16/2007
11	11	CPU Power & Ground	T9_NOME	03/16/2007
12	12	CPU Decoupling & VID	M76_MLB	03/19/2007
13	13	eXtended Debug Port (XDP)	T9_NOME	12/12/2006
14	14	NB CPU Interface	T9_NOME	03/16/2007
15	15	NB PEG / Video Interfaces	T9_NOME	03/16/2007
16	16	NB Misc Interfaces	T9_NOME	03/16/2007
17	17	NB DDR2 Interfaces	T9_NOME	03/16/2007
18	18	NB Power 1	T9_NOME	03/16/2007
19	19	NB Power 2	T9_NOME	03/16/2007
20	20	NB Grounds	T9_NOME	03/16/2007
21	21	NB Standard Decoupling	T9_NOME	01/17/2007
22	22	NB Graphics Decoupling	M76_MLB	03/12/2007
23	23	SB Enet, Disk, FSB, LPC	T9_NOME	03/16/2007
24	24	SB PCI, PCIe, DMI, USB	T9_NOME	03/16/2007
25	25	SB Pwr Mgt, GPIO, Clink	T9_NOME	03/16/2007
26	26	SB Power & Ground	T9_NOME	03/16/2007
27	27	SB Decoupling	T9_NOME	01/17/2007
28	28	SB Misc	(T9_MLB)	08/24/2006
29	29	Clock (CK505)	T9_NOME	03/16/2007
30	30	Clock Termination	(MASTER)	08/23/2006
31	31	DDR2 SO-DIMM Connector A	(M59_SYNC)	08/24/2006
32	32	DDR2 SO-DIMM Connector B	(M59_SYNC)	08/24/2006
33	33	Memory Active Termination	(T9_NOME)	11/14/2006
34	34	Left I/O Board Connector	(M59_SYNC)	08/24/2006
35	37	Ethernet (Yukon)	T9_NOME	03/16/2007
36	38	Yukon Power Control	T9_NOME	03/16/2007
37	39	Ethernet Connector	M76_MLB	03/19/2007
38	40	FireWire Link (TSB83AA22)	M76_MLB	03/19/2007
39	41	FireWire PHY (TSB83AA22)	M76_MLB	03/19/2007
40	42	FireWire Port Power	M76_MLB	03/19/2007
41	43	FireWire Ports	M76_MLB	03/19/2007
42	44	PATA Connector	(MASTER)	(MASTER)
43	46	External USB Connector	M76_MLB	03/19/2007
44	47	Left Clutch Barrel Interconnect	M76_MLB	03/19/2007
45	49	SMC	T9_NOME	01/17/2007
46	50	SMC Support	(MASTER)	(MASTER)
47	51	LPC+ Debug Connector	M76_MLB	03/19/2007
48	52	SMBus Connections	(MASTER)	(MASTER)
49	53	Current & Voltage Sensing	(MASTER)	(MASTER)
50	54	Current Sensing	(MASTER)	(MASTER)
51	55	Thermal Sensors	(MASTER)	(MASTER)
52	56	Fan Connectors	M76_MLB	03/19/2007
53	58	ALS Support	M76_MLB	03/19/2007
54	59	Sudden Motion Sensor (SMS)	M76_MLB	03/19/2007
55	61	SPI BootROM	T9_NOME	03/16/2007
56	69	PBus-In & Battery Connectors	(M59_SYNC)	09/09/2006
57	70	Power FETs	M76_MLB	03/19/2007
58	71	IMVP6 CPU VCore Regulator	M76_MLB	01/23/2007
59	72	IMVP6 NB Gfx Core Regulator	M76_MLB	03/19/2007
60	73	5V / 3.3V Power Supply	M76_MLB	03/19/2007
61	74	1.25V / 1.05V Power Supply	M76_MLB	03/12/2007
62	75	1.8V DDR2 Supply	M76_MLB	03/19/2007
63	76	1.5V Power Supply	M76_MLB	03/12/2007
64	77	FW PHY Power Supplies	M76_MLB	03/19/2007
65	78	3.425V G3Hot Supply & Power Control	(MASTER)	(MASTER)
66	80	NV G84M PCI-E	(MASTER)	(MASTER)
67	81	NV G84M Core/FB Power	(MASTER)	(MASTER)
68	82	NV G84M Frame Buffer I/F	(MASTER)	(MASTER)
69	84	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
70	85	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
71	86	NV G84M GPIO/MIO/Misc	(MASTER)	(MASTER)
72	87	GPU Straps	(MASTER)	(MASTER)
73	88	NV G84M Video Interfaces	(MASTER)	(MASTER)
74	89	GPU (G84M) Core Supply	(MASTER)	(MASTER)
75	90	LVDS Display Connector	(MASTER)	(MASTER)
76	94	DVI Display Connector	(MASTER)	(MASTER)
77	95	LVDS Interface Mux	(MASTER)	(MASTER)
78	96	Project Specific Connectors	(M59_SYNC)	08/24/2006
79	100	CPU/FSB Constraints	T9_NOME	01/17/2007
80	101	NB Constraints	T9_NOME	01/17/2007
81	102	Memory Constraints	T9_NOME	01/17/2007
82	103	SB Constraints (1 of 2)	T9_NOME	01/17/2007
83	104	SB Constraints (2 of 2)	T9_NOME	01/17/2007
84	105	Clock & SMC Constraints	T9_NOME	01/17/2007
85	106	FireWire Constraints	T9_NOME	01/17/2007
86	107	GPU (G84M) Constraints	(MASTER)	(MASTER)
87	108	Project Specific Constraints	(MASTER)	(MASTER)
88	109	PCB Rule Definitions	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7225	1	SCHEM,MLB,MBP15	SCH	CRITICAL	
820-2101	1	PCBF,MLB,MBP15	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 24 17:23:54 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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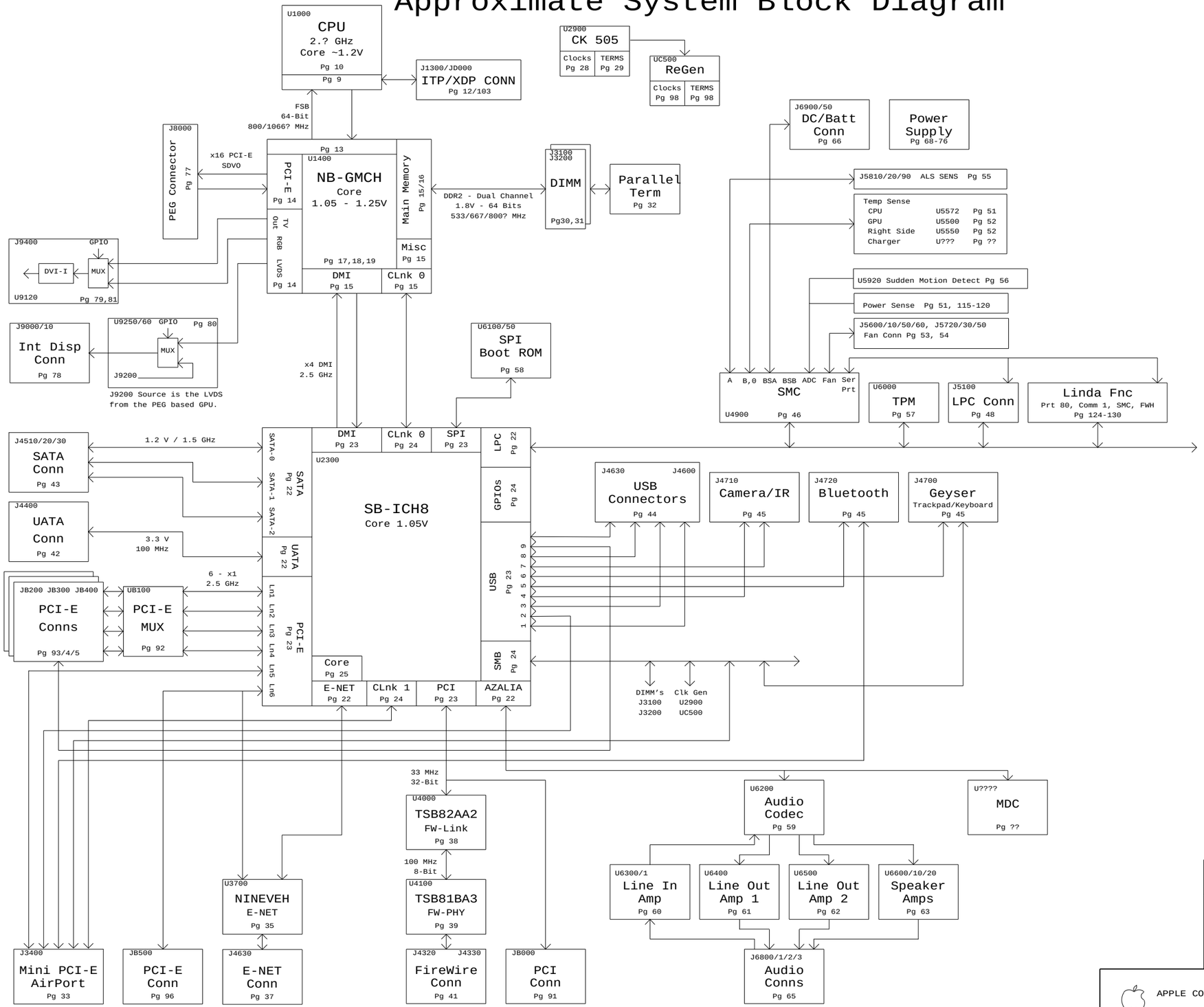
TITLE
SCHEM,MLB,MBP15

DRAWING NUMBER 051-7225 REV. A.0.0

SHT 1 OF 88

Approximate System Block Diagram



System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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SCALE NONE

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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D	051-7225	A.0.0
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Power Block Diagram

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D	051-7225	A.0.0
SCALE NONE	SHT 4 OF 88	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA,2.2GHZ,128SAM_VRAM,M75,MBP15	M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG
630-7932	PCBA,2.4GHZ,256SAM_VRAM,M75,MBP15	M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG
630-8659	PCBA,2.2GHZ,128HY_VRAM,M75,MBP15	M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX
630-8662	PCBA,2.4GHZ,256HY_VRAM,M75,MBP15	M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128,VRAM_SAMSUNG,VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128,VRAM_HYNIX,VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3464	1	IC,MDC,SR,E1,PRQ,2.2G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3465	1	IC,MDC,SR,E1,PRQ,2.4G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LW PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BI-Tech magnetics
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-7225	A.0.0
SCALE NONE	SHT 5 OF 88	

PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMOPTIONs and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMOPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMOPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONs to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT_SE

10.1.0:
01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes
10.2.0:
01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes
11.0.0:
01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0:
02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0:
02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0:
02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0:
02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
12.4.0:
03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0:
03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements
12.6.0:
03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0:
03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
15.0.0:
03/30/07 -- SIL: Changed R5031 to 2.21K and R5032 to 9.53K to raise SIL current approx 15% (lightpipe dimmed by 20%)
03/30/07 -- Power Supply: Changed 1.05V power supply current limit to 10A from 8A (R7455 to 5.62k -- rdar://5095642)
04/03/07 -- Power Supply: Changed numerous 10K Rs to 100K for Energy Star compliance (rdar://5102118)
04/03/07 -- GPU FB: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN
04/03/07 -- CPU Vcore: Changed R7117,C7134 and R7115,R7130 for calibration improvements (rdar://5085959)
04/03/07 -- Released for DVT (BOM update)
16.0.0:
04/17/07 -- Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive S5 enable pins directly
04/17/07 -- Released for DVT (As-Built)

PVT

16.1.0:
04/18/07 -- GPU Misc: Added R8735-37 to implement PCI DEVID 0x407 in hardware
16.2.0:
04/18/07 -- Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)
04/18/07 -- Modules: Updated Intel chipset to PRQ parts
16.3.0:
04/20/07 -- Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS
04/20/07 -- Power FETs: Changed C7095/C7083 to 16V for proper rating of parts tied to PBUS
04/20/07 -- CPU VCore: Changed C7196 to 16V to eliminate a BOM item
17.0.0:
04/20/07 -- No changes. Weekly BOM release.
A.0.0:
04/24/07 -- SB Decoupling: Changed L2700 from 155S0152 to 155S0333 for AVL updates
04/24/07 -- SMC Support: Changed R5031 to 2.37K, R5032 to 9.09K to meet SIL brightness targets
04/24/07 -- Released for PVT

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-7225	A.0.0

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Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 52
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	8 47
TRUE	=PP5V_S0_LPCPLUS	8 47
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	BOOT_LPC_SPI_L	24 47
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 84
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	8 78
TRUE	ALS_GAIN	45 53 78
TRUE	LTALS_OUT	53 78
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

1665 TRUE	HSTHMSNS_D_P	51 87
1666 TRUE	HSTHMSNS_D_N	51
TRUE	RSFSTHMSNS_D_P	51 87
TRUE	RSFSTHMSNS_D_N	51
	CPUTHMSNS_D2_P	51 87
	CPUTHMSNS_D2_N	51

CPUTHMSNS can not be supported due to layout constraints

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	45 46 56
TRUE	=SMBUS_BATT_SCL	48 56
TRUE	=SMBUS_BATT_SDA	48 56
TRUE	GND_BATT	56

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	8 56
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	45 49
TRUE	=PP5V_S0_ISENSECAL	8 49
TRUE	=PPVCORE_S0_NBGFX_REG	8 59
TRUE	=PPVCORE_S0_CPU_REG	8 49 58
TRUE	=PPVCORE_GPU_REG	8 49 74
TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	8 44
TRUE	USB_CAMERA_N	24 44 82
TRUE	USB_CAMERA_P	24 44 82
TRUE	=PP5V_S3_WWAN	8 44
TRUE	USB_WWAN_N	44
TRUE	USB_WWAN_P	44

Other Func Test Points

FUNC_TEST

TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 78

System Validation TPs

FUNC_TEST

TRUE	CPU_PWRGD	10 13 23 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_DPRSLPVR	16 25 58 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWROK	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGOOD_DELAY	9 16 28 58
TRUE	FSB_CPURST_L	10 13 14 79
TRUE	FSB_CPUSLP_L	10 14 79
TRUE	FSB_DPWR_L	10 14 79
TRUE	NB_SB_SYNC_L	16 25

FUNC_TEST

TRUE	IMVP_VR_ON	45 58
TRUE	IMVP_DPRSLPVR	58 79
TRUE	PM_SLP_S3_L	25 36 40 45 65
TRUE	PM_S4_STATE_L	25 45 65
TRUE	PM_SLP_S5_L	25 45 46
TRUE	PM_ENET_EN	36 65
TRUE	P1V5P1V05S0_PGOOD	65
TRUE	CPU_DPRSTP_L	10 16 23 58 79
TRUE	IMVP6_VID<6..0>	12 58 79
TRUE	PLT_RST_L	24 28 77
	NB_RESET_L	16 28
TRUE	GPU_RESET_L	28 66
TRUE	SMC_LRESET_L	28 45
TRUE	CPU_STPCLK_L	10 23 79
TRUE	FSB_CLK_NB_P	14 30 84
TRUE	FSB_CLK_NB_N	14 30 84
TRUE	NB_CLKREQ_L	16 29
TRUE	NB_CLK100M_PCIE_P	16 30 84
TRUE	NB_CLK100M_PCIE_N	16 30 84
TRUE	NB_CLK96M_DOT_P	84
TRUE	NB_CLK96M_DOT_N	84
TRUE	NB_CLK100M_DPLLSS_P	22 30 84
TRUE	NB_CLK100M_DPLLSS_N	22 30 84
TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 79
TRUE	FSB_ADS_L	10 14 79
TRUE	FSB_ADSTB_L<1..0>	10 14 79
TRUE	FSB_BNR_L	10 14 79
TRUE	FSB_BREQ0_L	10 14 79
TRUE	FSB_D_L<63..0>	10 14 79
TRUE	FSB_DBSY_L	10 14 79
TRUE	FSB_DINV_L<3..0>	10 14 79
TRUE	FSB_DRDY_L	10 14 79
TRUE	FSB_DSTB_L_N<3..0>	10 14 79
TRUE	FSB_DSTB_L_P<3..0>	10 14 79
TRUE	FSB_HIT_L	10 14 79
TRUE	FSB_HITM_L	10 14 79
TRUE	FSB_LOCK_L	10 14 79
TRUE	FSB_REQ_L<4..0>	10 14 79

GPU NO_TESTs

NO_TEST

1570 TRUE	LVDS_L_DATA_N<1>	73 77 86
1571 TRUE	LVDS_L_DATA_N<2>	73 77 86
1572 TRUE	LVDS_L_DATA_P<2>	73 77 86

NB NO_TESTs

NO_TEST

TRUE	NC_NB_NC<1..16> = TP_NB_NC<1..16>	16

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
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"G3Hot" (Always-Present) Rails

56 7 =PPBUS_G3H_LIO_CONN — PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12V
MAKE_BASE=TRUE
- =PPBUS_S5_FWPWRSW 40
- =PPBUS_S5_P1V8GPUFET 57
- =PPBUS_S5_P1V25S0FET 57
- =PPVIN_S5_CPU_IMVP_VIN 58
- =PPVIN_S5_CPU_IMVP 58
- =PPVIN_S5_P5VP3V3 60
- =PPVIN_S5_P5VS5 60
- =PPVIN_S5_P3V3S5 60
- =PPVIN_ENET_P1V25ENET 61
- =PPVIN_S3_P1V8S3 62
- =PPVIN_S0_P1V5S0 63
- =PPVIN_S0_GFXIMVP6 59
- =PPVIN_S0_P1V05S0 61
- =PPVIN_GPU_GPUVCORE 74

34 =PPDCIN_G3H_LIO_CONN — PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPVIN_G3H_P3V42G3H 65

65 =PP3V42_G3H_REG — PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SB_RTC 28
- =PP3V42_G3H_LIO 34
- =PP3V42_G3H_SMCUSBMUX 43
- =PP3V42_G3H_SMBUS_SMC_BSA 48
- =PP3V42_G3H_LIDSWITCH 78
- =PP3V3_S5_SMC 45 46
- =PP3V3_S5_LPCPLUS 7 47
- =PPVIN_S5_SMCVREF 46
- =PP3V42_G3H_PWRCTL 65

5V Rails

60 =PP5V_S5_REG — PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_SB 27
- =PP5V_S5_P1V8GPUFET 57
- =PP5V_S5_P1V8S0FET 57
- =PP5V_S5_P1V25GPUFET 57
- =PP5V_S5_P1V25S0FETXW 9
- =PP5V_S5_P1V25ENET 61
- =PP5V_S5_P1V05S0 61
- =PP5V_S5_P1V8DDRREG 62
- =PP5V_S5_P1V5S0 63
- =PP5V_S5_PWRCTL 65
- =PP5V_S5_GPUVCORE 74
- =PP5V_S3_RTUSB 43
- =PP5V_S3_P5VS3FET 57
- =PP5V_S0_P5VS0FET 57

57 =PP5V_S3_FET — PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED 46
- =PP5V_S3_CAMERA 7 44
- =PP5V_S3_WWAN 7 44
- =PP5V_S3_IR 78
- =PP5V_S3_TOPCASE 78
- =PP5V_S0_KBDLED 53
- =PP5V_S0_ISENSECAL 7 49

57 =PP5V_S0_FET — PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_SB 27
- =PP5V_S0_ODD 42
- =PP5V_S0_LPCPLUS 7 47
- =PP5V_S0_FAN_LT 7 52
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_CPU_IMVP 58
- =PP5V_S0_GFXIMVP6 59
- =PP5V_S0_DVI_DDC 76
- =PP5V_S0_SB_HPD 76
- =PP5V_S0_HDD 78
- =PP5V_S0_ODDPWREN 42
- =PP5V_S0_PCIREQFIX 42

Chipset "VCore" Rails

58 49 7 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 11 12 49

59 7 =PPVCORE_S0_NBGFX_REG — PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB_GFX 18 22
- =PPVCORE_S0_NBGFX_VSEN 59

3.3V-2.5V Rails

60 =PP3V3_S5_REG — PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S5_SB_PM 28
- =PP3V3_S5_SB_USB 24
- =PP3V3_S5_SB 25 27
- =PP3V3_S5_SB_CLINK1 25
- =PP3V3_S5_SB_GPIO 25
- =PP3V3_S5_SB_3V3_VCCSUSHDA 26 27
- =PP3V3_S5_SB_VCCSUS3_3 26 27
- =PP3V3_S5_SB_VCCSUS3_3_USB 26 27
- =PP3V3_S5_S5PWRGD 46
- =PP3V3_S5_SMBUS_SB_ME 48
- =PP3V3_S5_ROM 55
- =PP3V3_S5_P1V5P1V05PG 65
- =PP3V3_S3_P3V3S3FET 57
- =PP3V3_S0_LCD 75
- =PP3V3_S0_P3V3S0FET 57
- =PP3V3_GPU_P3V3GPUFET 57
- =PP3V3_S5_PWRCTL 65

57 =PP3V3_S3_FET — PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S3_P3V3ENETFET 36
- =PP3V3_S3_FW 38
- =PP3V3_S3_PCI 38
- =PP3V3_S3_SMBUS_SMC_A_S3 48
- =PP3V3_S3_RTALS 53
- =PP3V3_S3_SMS 54
- =PP3V3_S3_SMBUS_SMC_MGMT 48
- =PP3V3_S3_P1V25ISNS 50
- =PP3V3_S3_P1V8ISNS 50
- =PP3V3_S3_LTALS 7 78
- =PP3V3_S3_TOPCASE 78
- =PP3V3_S3_REMTHMSNS 51

57 =PP3V3_S0_FET — PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_NB_VCCHV 16 19 21
- =PP3V3_S0_NB_VCCA_PEG_BG 19 21
- =PP3V3_S0_NB_FOLLOW 21
- =PP3V3_S0_SB_GPIO 23 25
- =PP3V3_S0_SB_PCI 24
- =PP3V3_S0_SB_VCC3_3_IDE 26 27
- =PP3V3_S0_SB_VCC3_3_PCI 26 27
- =PP3V3R1V5_S0_SB_VCCHDA 26 27
- =PP3V3_S0_SB_VCC3_3_DMI 26 27
- =PP3V3_S0_SB_VCC3_3_VCCPCORE 26
- =PP3V3_S0_SB_VCCGLAN3_3 26
- =PP3V3_S0_SB_VCC3_3_SATA 26 27
- =PP3V3_S0_SB 27
- =PP3V3_S0_SB_PM 28
- =PP3V3_S0_RSTBUF 28
- =PP3V3_S0_CK505 29 30
- =PP3V3_S0_IDE 42
- =PP3V3_S0_SMC 46
- =PP3V3_S0_LPCPLUS 47
- =PP3V3_S0_SMBUS_SB 48
- =PP3V3_S0_SMBUS_SMC_B_S0 48
- =PP3V3_S0_CPUCOREISNS 50
- =PP3V3_S0_NBGFXCOREISNS 50
- =PP3V3_S0_CPUTHMSNS 51
- =PP3V3_S0_GPUTHMSNS 51
- =PP3V3_S0_FAN_LT 52
- =PP3V3_S0_FAN_RT 52
- =PP3V3_S0_IMVP 58
- =PP3V3_S0_GFXIMVP6 59
- =PP3V3_S0_NBCOREISNS 50
- =PP3V3_S0_ALLSYSPG 65
- =PP3V3_S0_DDC_LCD 75
- =PP3V3_S0_LVDS_MUX 77
- =PP3V3R5V_GPU_GPUISENS 74
- =PP3V3_S0_XDP 13
- =PP3V3_S0M_CK505 29 30
- =PP3V3_S0_GPUCLKGATE 30
- =PPSPD_S0M_MEM_A 31
- =PPSPD_S0M_MEM_B 32
- =PP3V3_S0MWOL_SB_CLINK0 25
- =PP3V3_S0MWOL_SB_VCCCL3_3 26 27
- =PP3V3_S0MWOL_SB_VCCLAN3_3 26 27
- =PP3V3_S0_PWRCTL 65

59 =PP1V25_ENET_ISNS — PP1V25_ENET_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0_P1V25S0FET 57
- =PP1V25_GPU_P1V25GPUFET 57

1.8V-0.9V Rails

62 =PP1V8_S3_REG — PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3_FW 38
- =PP1V8_S3M_MEM_A 31 87
- =PP1V8_S3M_MEM_B 32 87
- =PP1V8_S3_ISNS_R 50
- =PP1V8_GPU_P1V8GPUFET 57

50 =PP1V8_S3_ISNS — PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3M_NB_VCC 21
- =PP1V8_S3M_MEM_NB 16 18 21
- =PP1V8_S0_P1V8S0FET 57

57 =PP1V8_S0_FET — PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
MAX I = 0.36A
- =PP1V8_S0_NB_LVDS 22
- =PPVIN_S0_NB_DPLL 22

63 =PP1V5_S0_REG — PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
MAX I = ?.??A
- =PP1V5_S0_CPU 11 12
- =PP1V5_S0_NB_TVDAC 22
- =PP1V5_S0_SB 27
- =PP1V5_S0_SB_VCC1_5_A_ARX 26 27
- =PP1V5_S0_SB_VCC1_5_A_ATX 26 27
- =PP1V5_S0_SB_VCC1_5_A 26
- =PP1V5_S0_SB_VCCUSBPLL 26 27
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE 26 27
- =PP1V5_S0_LIO 34

57 =PP1V25_S0_FET — PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0M_NB_PLL 21
- =PP1V25_S0M_NB_VCC 21
- =PP1V25_S0M_NB_VCCA 21
- =PP1V25_S0_NB_VCCDMI 19 21
- =PP1V25_S0_NB_PLL 21
- =PP1V25_S0_NB_VCC 21
- =PP1V25_S0_SB_DMI 26 27

61 =PP1V05_S0_REG — PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0M_NB_VCCAXM 18 21
- =PP1V05_S0_CPU 10 11 12 13
- =PP1V05_S0_NB_FOLLOW 21
- =PP1V05_S0_NB_PCIE 21
- =PP1V05_S0_SB_CPU_IO 23 26 27
- =PP1V05_S0_SMC_LS 46
- =PP1V25R1V05_S0_FSB_NB 14 30
- =PP1V25R1V05_S0_NB_VTT 19 21
- =PPVCORE_S0_NBCOREISNS 50
- =PPVCORE_S0_NB_FOLLOW 21
- =PPVCORE_S0_SB 26 27

50 =PPVCORE_S0_NB_R — PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB 18 21 22

62 =PP0V9_S3_VTTR_BUF — PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S3M_MEM_NBVREFA 16
- =PP0V9_S3M_MEM_NBVREFB 16
- =PP0V9_S3M_MEM_DIMMVREFA 31
- =PP0V9_S3M_MEM_DIMMVREFB 32

62 =PP0V9_S0_VTT_LDO — PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S0M_MEM_TERM 33

"ENET" Rails

36 =PP3V3_ENET_FET — PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_ENET_PHY 35
- =PP3V3_ENET_AVDDLDO 36

36 =PPVOUT_ENET_AVDDLDO — PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
- =PP1V8R2V5_ENET_PHY 35

61 =PP1V25_ENET_REG — PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_ENET_PHY 35
- =PP1V25_ENET_ISNS_R 50

=YUKON_EC_PP2V5_ENET 35
Yukon EC will not be supported

"FW" (FireWire) Rails

40 PPBUS_FW_FWPWRSW_F — =PPBU_S0_P3V3FW 64
MAKE_BASE=TRUE

40 =PPBUS_S5_FW_FET — PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVP_FW_SUMNODE 40
- =PPVP_FW_CPS 39
- =PPVP_FW_P3V3FW 64

40 PPVP_FW_PORTA_UF — =PPVP_FW_PORT0 41
MAKE_BASE=TRUE
40 PPVP_FW_PORTB_UF — =PPVP_FW_PORT1 41
MAKE_BASE=TRUE

64 =PP3V3_FW_REG — PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_PHY 39 41
- =PP3V3_FW_LATEVG_ACTIVE 40
- =PP3V3_FW_LATEVG 41
- =PPVIN_FW_P1V95FW 64

64 =PP1V95_FW_LDO — PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
- =PP1V95_FW_PHY 39
- =PP1V8_FW_PHYOSC 39

"GPU" Rails

57 =PP3V3_GPU_FET — PP3V3_GPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_VDD33 71
- =PP3V3_GPU_MIO 71 72
- =PP3V3_GPU_DAC 73
- =PP3V3_GPU_DVI 76
- =PP3V3_GPU_LVDS_DDC 77
- =PP3V3_GPU_VGASYNC 76
- =PP3V3_GPU_TMDS 72
- =PP3V3_GPU_VIDEOMUX 72
- =PP2V5_GPU_LTC2900 77
- =PP3V3_GPU_SMBUS_SMC_0_S0 48
- =PP3V3_GPU_PWRCTL 65
- =PP3V3_GPU_VCORELOGIC 74
- =PP3V3_GPU_HDCP 72

72 =PP3V3_GPU_TMDS_FET — PP3V3_GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_TMDSBIAS 76
- =PP3V3_GPU_IFPCD_IOVDD 73

57 =PP1V8_GPU_FET — PP1V8_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_FB_VDD 69 70
- =PP1V8_GPU_FB_VDDQ 69 70
- =PP1V8_GPU_FBVDDQ 67
- =PP1V8_GPU_FBIO 68
- =PP1V8_GPU_IFPX 73

57 =PP1V25_GPU_FET — PP1V25_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_GPU_PEX_IOVDDQ 66
- =PP1V2_GPU_PEX_IOVDD 66
- =PP1V2_GPU_PEX_PLLXVDD 66
- =PP1V2_GPU_PLLVDD 71
- =PP1V2_GPU_H_PLLVDD 71
- =PP1V2_GPU_VID_PLLVDD 71
- =PP1V2_GPU_FBPLLAVDD 68
- =PP1V2_GPU_VCOREPWRCTL 74

74 49 7 =PPVCORE_GPU_REG — PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PPVCORE_GPU 67

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Thermal Module Holes

Top CPU TM Notch
Add 2 buried vias to GND

ZT0985 5P75R2P7 — Top GPU Right TM Hole

ZT0970 5P75R2P7 — Left CPU TM Hole

ZT0975 5P75R2P7 — Right CPU TM Hole

ZT0980 5P75R2P7 — Bottom Left GPU TM Hole

RAM Door (Torx) Holes

ZT0930 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_0

ZT0935 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_1

Frame Holes

ZT0920 3P2R2P7 — GND_CHASSIS_LVDS_HOLE

ZT0940 3P7R3P2 — GND_CHASSIS_RIGHT_FAN_HOLE

Board Edge Notches (Can't be PTH)

ZT0945 HOLE-VIA-P5RP25 — GND_CHASSIS_RIGHT_FAN_NOTCH

ZT0950 HOLE-VIA-P5RP25 — GND_CHASSIS_DIMM_NOTCH

ZT0955 3P2R2P7 — GND_CHASSIS_LIOFLEX_HOLE

ZT0965 3P2R2P7 — GND_CHASSIS_LINDACARD_HOLE

Tooling Holes (Can't be PTH)

ZT0960 HOLE-VIA-P5RP25 — GND_CHASSIS_BATTCONN_HOLE

ZT0990 HOLE-VIA-P5RP25 — GND_CHASSIS_DVI_HOLE

Chassis GNDs

GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI_TOP (76)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI_BOT (76)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

OMIT R0910 SHORT NONE NONE NONE 402

GND_CHASSIS_ENET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_ENET (37)
=GND_CHASSIS_FW_PORT1 (41)
=GND_CHASSIS_FW_PORT0U (41)

GND_CHASSIS_RTUSB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_FW_PORT0L (41)
=GND_CHASSIS_RTUSB (43)

SH0925 0G-503040 SHLD-SM-LF

GND_CHASSIS_LEFTCLUTCH
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_LEFTCLUTCH (44)
=GND_CHASSIS_J5590 (51)

PM_SB_PWROK (28 25 7) MAKE_BASE=TRUE — =SB_CLINK_MPWROK (25)
VR_PWRGOOD_DELAY (58 28 16 7) MAKE_BASE=TRUE — =NB_CLINK_MPWROK (16)
SMC_SMS_INT (54) MAKE_BASE=TRUE — =SMC_SMS_INT (45)
PEG_CLK100M_GPU_P (66 30) MAKE_BASE=TRUE — PEG_CLK100M_P (84)
PEG_CLK100M_GPU_N (66 30) MAKE_BASE=TRUE — PEG_CLK100M_N (84)
PM_ALL_NBGFX_PGOOD (77) MAKE_BASE=TRUE — GFXIMVP6_PGOOD (59)
GFX_VR_EN (59) MAKE_BASE=TRUE — =GFX_VR_EN (16)
GFXIMVP6_VID<4..0> (59) MAKE_BASE=TRUE — GFX_VID<4..0> (16)
TP_MEM_A_A<15> MAKE_BASE=TRUE — MEM_A_A<15> (31)
TP_MEM_B_A<15> MAKE_BASE=TRUE — MEM_B_A<15> (32)
TP_USB_EXTCP MAKE_BASE=TRUE — USB_EXTC_P (24 82)
TP_USB_EXTCN MAKE_BASE=TRUE — USB_EXTC_N (24 82)

XW0900 SM
(8) =PP5V_S5_P1V25S0FETXW — 1 — 2 — PP5V_S5_P1V25S0FET (57) — =PP5V_S5_P1V25S0FET
MIN_LINE_WIDTH=0.1 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5V
MAKE_BASE=TRUE
NO_TEST=TRUE

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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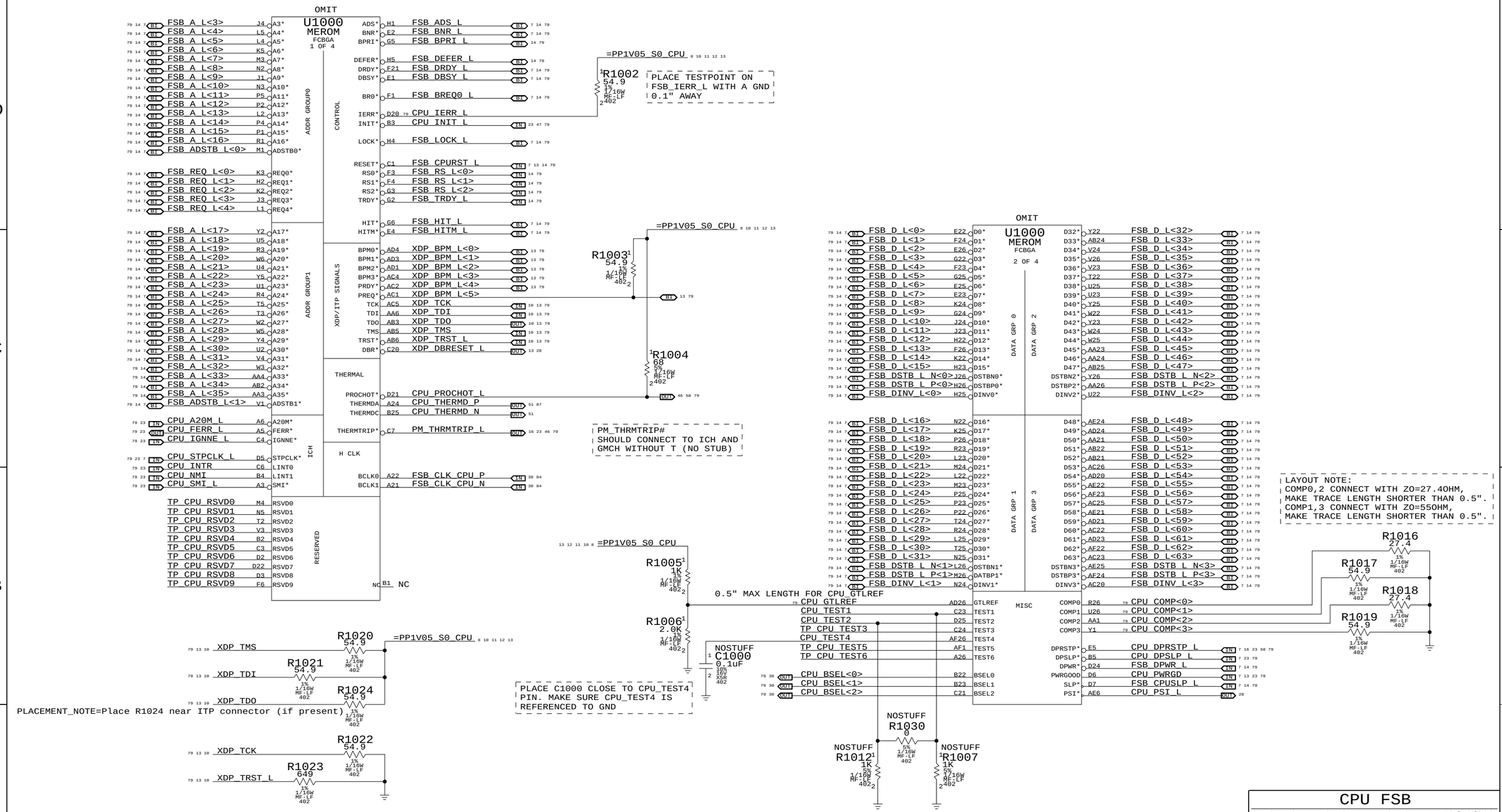

CPU FSB

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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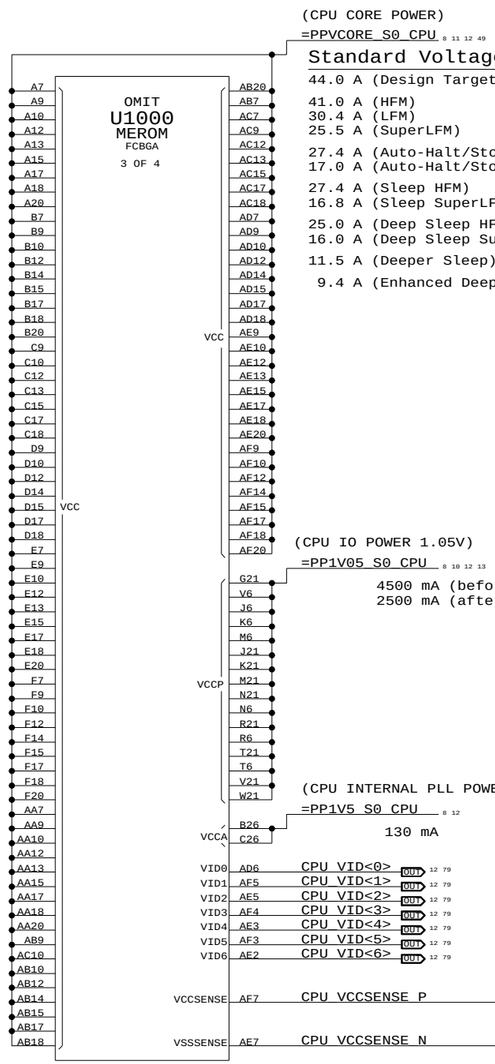
SCALE NONE	SHT 10 OF 88	



(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

CPU_VID<0> OUT 12 79
CPU_VID<1> OUT 12 79
CPU_VID<2> OUT 12 79
CPU_VID<3> OUT 12 79
CPU_VID<4> OUT 12 79
CPU_VID<5> OUT 12 79
CPU_VID<6> OUT 12 79

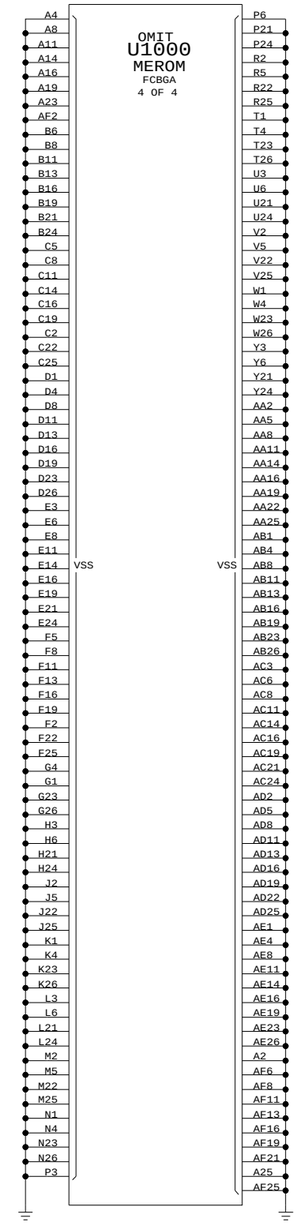
CPU_VCCSENSE_P OUT 58 79

CPU_VCCSENSE_N OUT 58 79

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.



Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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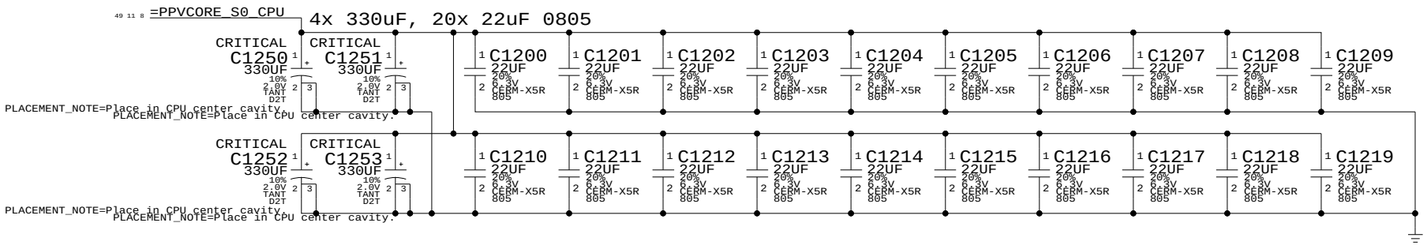
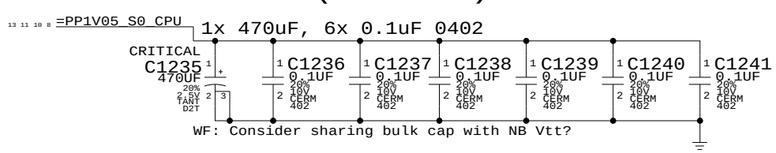
CPU VCORE HF AND BULK DECOUPLING

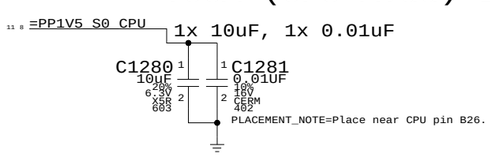


CPU VCORE VID CONNECTIONS

VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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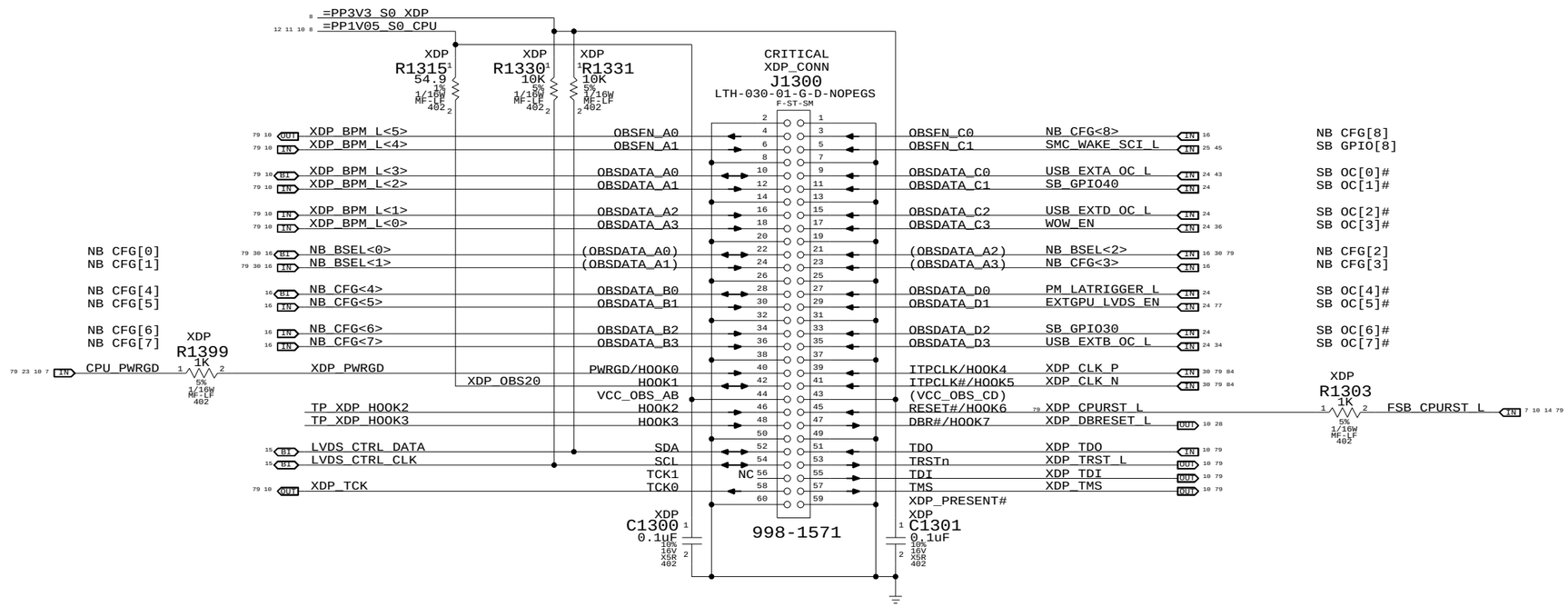
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

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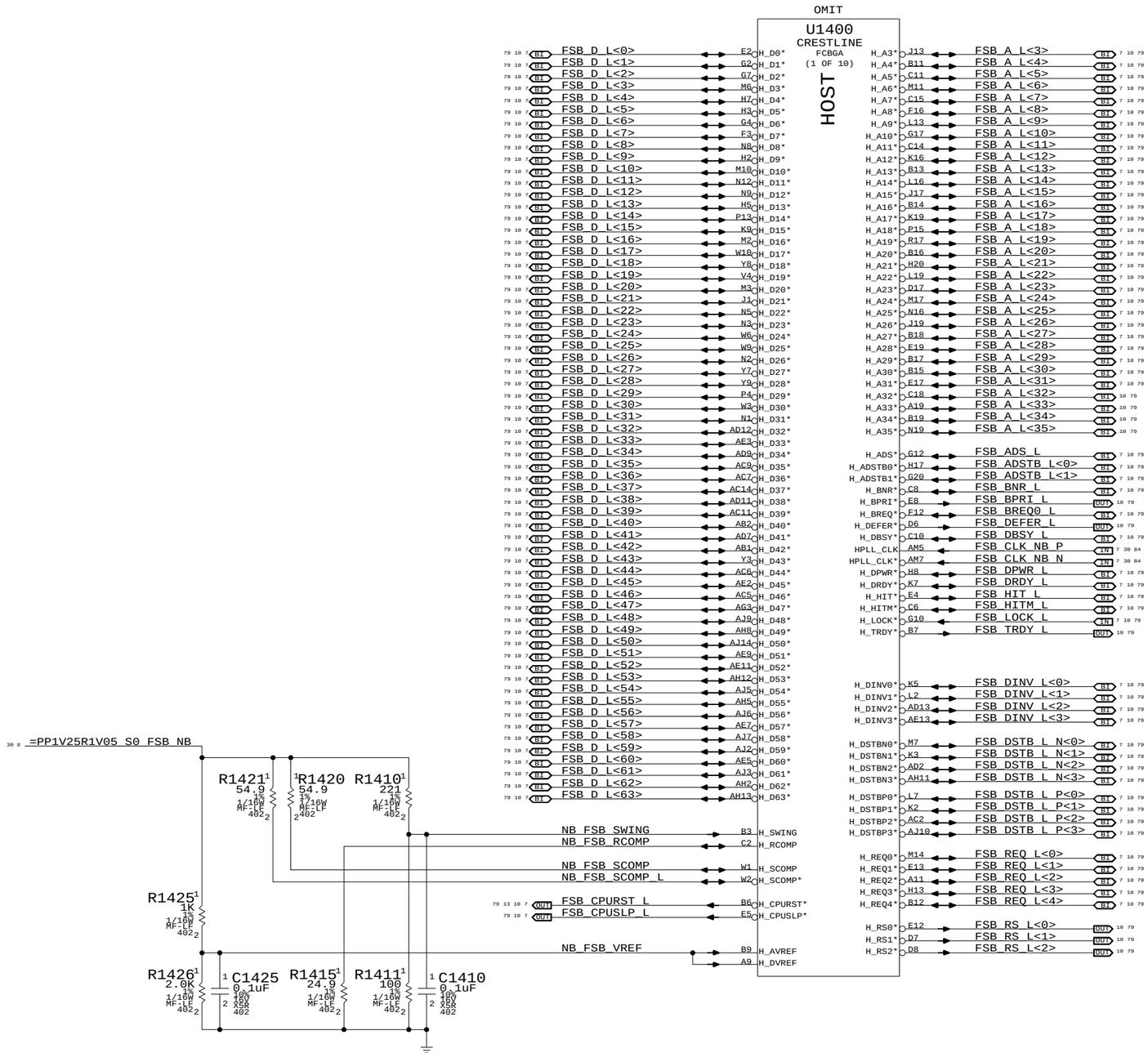

NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE NONE | SHT 14 OF 88

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

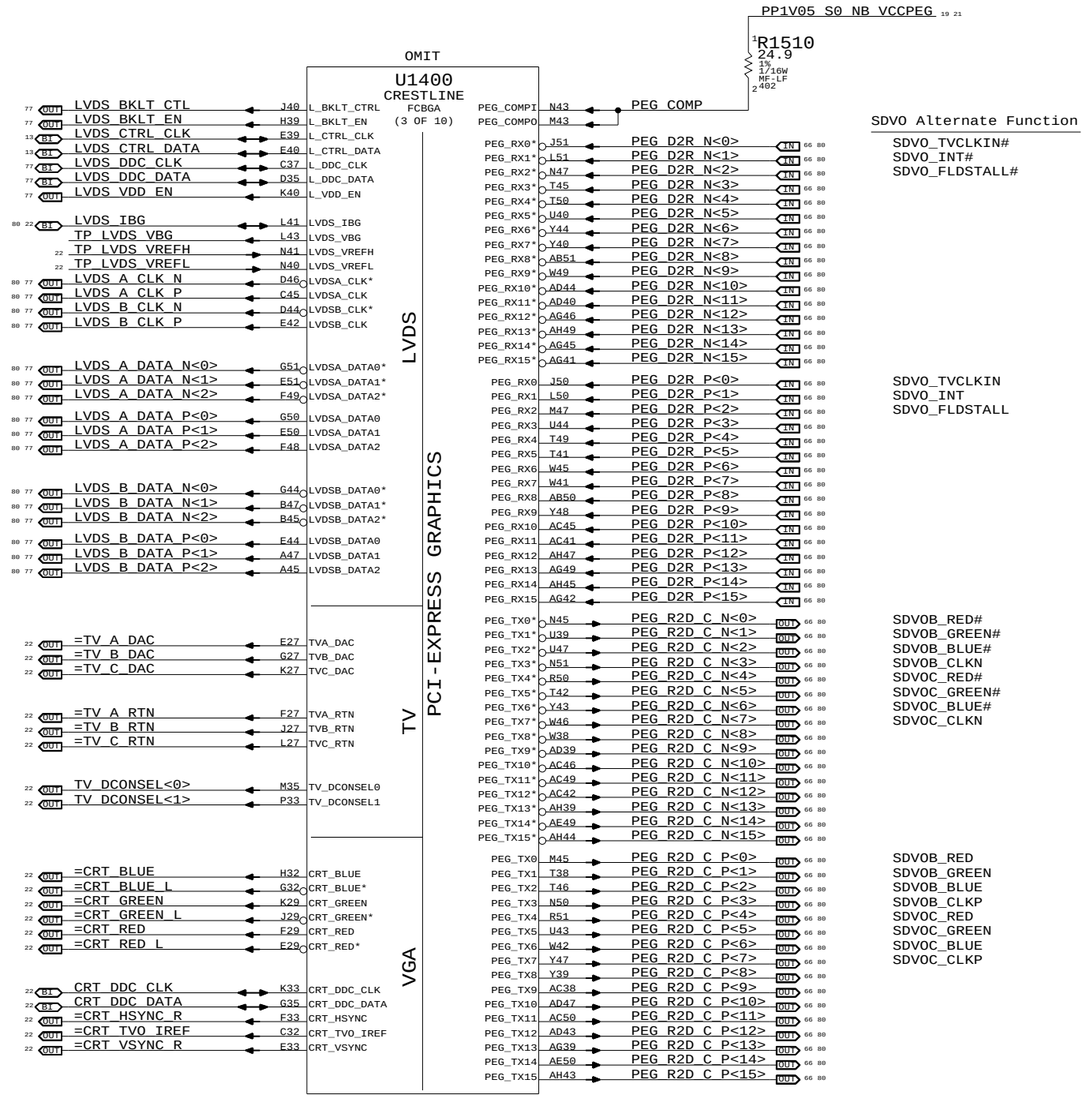
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
45 31 IN PM_EXTTS_L<0>
45 32 IN PM_EXTTS_L<1>

OMIT
U1400
CRESTLINE
FCBGA
(2 OF 10)

RSVD

TP_NB_RSVD<1>	P36	RSVD1	
TP_NB_RSVD<2>	P37	RSVD2	
TP_NB_RSVD<3>	R35	RSVD3	
TP_NB_RSVD<4>	N35	RSVD4	
TP_NB_RSVD<5>	AR12	RSVD5	
TP_NB_RSVD<6>	AR13	RSVD6	
TP_NB_RSVD<7>	AM12	RSVD7	
TP_NB_RSVD<8>	AN13	RSVD8	
TP_NB_RSVD<9>	J12	RSVD9	
TP_NB_RSVD<10>	AR37	RSVD10	
TP_NB_RSVD<11>	AM36	RSVD11	
TP_NB_RSVD<12>	AL36	RSVD12	
TP_NB_RSVD<13>	AM37	RSVD13	
TP_NB_RSVD<14>	D20	RSVD14	
TP_NB_RSVD<20>	H10	RSVD20	
TP_NB_RSVD<21>	B51	RSVD21	
TP_NB_RSVD<22>	BJ20	RSVD22	
TP_NB_RSVD<23>	BK22	RSVD23	
TP_NB_RSVD<24>	BF19	RSVD24	
TP_NB_RSVD<25>	BH20	RSVD25	
TP_NB_RSVD<26>	BK18	RSVD26	
TP_NB_RSVD<27>	BJ18	RSVD27	
TP_MEM_CLKP2	BF23	SM_CK2	
TP_MEM_CLKN2	BG23	SM_CK2*	
TP_MEM_CLKP5	BC23	SM_CK5	
TP_MEM_CLKN5	BD24	SM_CK5*	
81 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14	
81 33 32 OUT MEM_B_A<14>	BE24	SB_MA14	
TP_NB_RSVD<34>	BH39	RSVD34	
TP_NB_RSVD<35>	AW20	RSVD35	
TP_NB_RSVD<36>	BK20	RSVD36	
TP_LVDS_A_DATAN3	C48	RSVD37	
TP_LVDS_A_DATAP3	D47	RSVD38	
TP_LVDS_B_DATAN3	B44	RSVD39	
TP_LVDS_B_DATAP3	C44	RSVD40	
TP_NB_RSVD<41>	A35	RSVD41	
TP_NB_RSVD<42>	B37	RSVD42	
TP_NB_RSVD<43>	B36	RSVD43	
TP_NB_RSVD<44>	B34	RSVD44	
TP_NB_RSVD<45>	C34	RSVD45	

CFG

79 30 13 IN NB_BSEL<0>	P27	CFG0	
79 30 13 IN NB_BSEL<1>	N27	CFG1	
79 30 13 IN NB_BSEL<2>	N24	CFG2	
13 OUT NB_CFG<3>	C21	CFG3	IPU
13 BI NB_CFG<4>	C23	CFG4	IPU
16 13 BI NB_CFG<5>	F23	CFG5	IPU
13 OUT NB_CFG<6>	N23	CFG6	IPU
13 OUT NB_CFG<7>	G23	CFG7	IPU
13 OUT NB_CFG<8>	J20	CFG8	IPU
16 NB_CFG<9>	C20	CFG9	IPU
TP_NB_CFG<10>	R24	CFG10	IPU
TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	J23	CFG12	IPU
TP_NB_CFG<13>	E23	CFG13	IPU
TP_NB_CFG<14>	E20	CFG14	IPU
TP_NB_CFG<15>	K23	CFG15	IPU
16 NB_CFG<16>	M20	CFG16	IPU
TP_NB_CFG<17>	M24	CFG17	IPU
TP_NB_CFG<18>	L32	CFG18	IPD
16 NB_CFG<19>	N33	CFG19	IPD
16 NB_CFG<20>	L35	CFG20	IPD

PM

25 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*
79 58 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*
	L36	PM_EXT_TS0*
	J36	PM_EXT_TS1*
58 28 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK
28 7 IN NB_RESET_L	AV20	RSTIN*
79 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*
79 58 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR

NC

7 TP_NB_NC<1>	BJ51 NC1
7 TP_NB_NC<2>	BK51 NC2
7 TP_NB_NC<3>	BK50 NC3
7 TP_NB_NC<4>	BL50 NC4
7 TP_NB_NC<5>	BL49 NC5
7 TP_NB_NC<6>	BL3 NC6
7 TP_NB_NC<7>	BL2 NC7
7 TP_NB_NC<8>	BK1 NC8
7 TP_NB_NC<9>	BJ1 NC9
7 TP_NB_NC<10>	E1 NC10
7 TP_NB_NC<11>	A5 NC11
7 TP_NB_NC<12>	C51 NC12
7 TP_NB_NC<13>	B50 NC13
7 TP_NB_NC<14>	A50 NC14
7 TP_NB_NC<15>	A49 NC15
7 TP_NB_NC<16>	BK2 NC16

DDR MUXING

SM_CK0	AV29	MEM_CLK_P<0> (OUT 31 81)
SM_CK1	BB23	MEM_CLK_P<1> (OUT 31 81)
SM_CK3	BA25	MEM_CLK_P<3> (OUT 32 81)
SM_CK4	AV23	MEM_CLK_P<4> (OUT 32 81)
SM_CK0*	AW30	MEM_CLK_N<0> (OUT 31 81)
SM_CK1*	BA23	MEM_CLK_N<1> (OUT 31 81)
SM_CK3*	AW25	MEM_CLK_N<3> (OUT 32 81)
SM_CK4*	AW23	MEM_CLK_N<4> (OUT 32 81)
SM_CKE0	BE29	MEM_CKE<0> (OUT 31 33 81)
SM_CKE1	AY32	MEM_CKE<1> (OUT 31 33 81)
SM_CKE3	BD39	MEM_CKE<3> (OUT 32 33 81)
SM_CKE4	BG37	MEM_CKE<4> (OUT 32 33 81)
SM_CS0*	BG20	MEM_CS_L<0> (OUT 31 33 81)
SM_CS1*	BK16	MEM_CS_L<1> (OUT 31 33 81)
SM_CS2*	BG16	MEM_CS_L<2> (OUT 32 33 81)
SM_CS3*	BE13	MEM_CS_L<3> (OUT 32 33 81)
SM_ODT0	BH18	MEM_ODT<0> (OUT 31 33 81)
SM_ODT1	BJ15	MEM_ODT<1> (OUT 31 33 81)
SM_ODT2	BJ14	MEM_ODT<2> (OUT 32 33 81)
SM_ODT3	BE16	MEM_ODT<3> (OUT 32 33 81)
SM_RCOMP	BL15	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA (IN 8)
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB (IN 8)

CLK

DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P (IN 22)
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N (IN 22)
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P (IN 22)
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N (IN 22)
PEG_CLK	K44	NB_CLK100M_PCIE_P (IN 7 30 84)
PEG_CLK*	K45	NB_CLK100M_PCIE_N (IN 7 30 84)

Clk used for PEG and DMI

DMI

DMI_RXN0	AN47	DMI_S2N_N<0> (IN 24 80)
DMI_RXN1	AJ38	DMI_S2N_N<1> (IN 24 80)
DMI_RXN2	AN42	DMI_S2N_N<2> (IN 24 80)
DMI_RXN3	AN46	DMI_S2N_N<3> (IN 24 80)
DMI_RXP0	AM47	DMI_S2N_P<0> (IN 24 80)
DMI_RXP1	AJ39	DMI_S2N_P<1> (IN 24 80)
DMI_RXP2	AN41	DMI_S2N_P<2> (IN 24 80)
DMI_RXP3	AN45	DMI_S2N_P<3> (IN 24 80)
DMI_TXN0	AJ46	DMI_N2S_N<0> (OUT 24 80)
DMI_TXN1	AJ41	DMI_N2S_N<1> (OUT 24 80)
DMI_TXN2	AM40	DMI_N2S_N<2> (OUT 24 80)
DMI_TXN3	AM44	DMI_N2S_N<3> (OUT 24 80)
DMI_TXP0	AJ47	DMI_N2S_P<0> (OUT 24 80)
DMI_TXP1	AJ42	DMI_N2S_P<1> (OUT 24 80)
DMI_TXP2	AM39	DMI_N2S_P<2> (OUT 24 80)
DMI_TXP3	AM43	DMI_N2S_P<3> (OUT 24 80)

GRAPHICS VID

GFX_VID0	E35	GFX_VID<0> (OUT 9)
GFX_VID1	A39	GFX_VID<1> (OUT 9)
GFX_VID2	C38	GFX_VID<2> (OUT 9)
GFX_VID3	B39	GFX_VID<3> (OUT 9)
GFX_VR_EN	E36	GFX_VID<4> (OUT 9)
		=GFX_VR_EN (OUT 9)

ME

CL_CLK	AM49	CLINK_NB_CLK (BI 25 83)
CL_DATA	AK50	CLINK_NB_DATA (BI 25 83)
CL_PWROK	AT43	=NB_CLINK_MPWROK (IN 9)
CL_RST*	AN49	CLINK_NB_RESET_L (OUT 25 83)
CL_VREF	AM50	83 NB_CLINK_VREF

MISC

SDVO_CTRL_CLK	H35	SDVO_CTRLCLK (BI 22)
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA (BI 22)
CLKREQ*	G39	NB_CLKREQ_L (OUT 7 29)
ICH_SYNC*	G40	NB_SB_SYNC_L (OUT 7 25)
TEST1	A37	NB_TEST1
TEST2	R32	NB_TEST2

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

21 18 8 =PP1V8_S3M_MEM_NB
R1610 20 1% 1/10W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/10W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/16W MF-LF 402
C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AR43	SA_DQ0	
MEM_A_DQ<1>	AW44	SA_DQ1	
MEM_A_DQ<2>	BA45	SA_DQ2	
MEM_A_DQ<3>	AY46	SA_DQ3	
MEM_A_DQ<4>	AR41	SA_DQ4	
MEM_A_DQ<5>	AR45	SA_DQ5	
MEM_A_DQ<6>	AT42	SA_DQ6	
MEM_A_DQ<7>	AW47	SA_DQ7	
MEM_A_DQ<8>	BB45	SA_DQ8	
MEM_A_DQ<9>	BF48	SA_DQ9	
MEM_A_DQ<10>	BG47	SA_DQ10	
MEM_A_DQ<11>	BJ45	SA_DQ11	
MEM_A_DQ<12>	BB47	SA_DQ12	
MEM_A_DQ<13>	BG50	SA_DQ13	
MEM_A_DQ<14>	BH49	SA_DQ14	
MEM_A_DQ<15>	BE45	SA_DQ15	
MEM_A_DQ<16>	AW43	SA_DQ16	
MEM_A_DQ<17>	BE44	SA_DQ17	
MEM_A_DQ<18>	BG42	SA_DQ18	
MEM_A_DQ<19>	BE40	SA_DQ19	
MEM_A_DQ<20>	BF44	SA_DQ20	
MEM_A_DQ<21>	BH45	SA_DQ21	
MEM_A_DQ<22>	BG40	SA_DQ22	
MEM_A_DQ<23>	BF40	SA_DQ23	
MEM_A_DQ<24>	AR40	SA_DQ24	
MEM_A_DQ<25>	AW40	SA_DQ25	
MEM_A_DQ<26>	AT39	SA_DQ26	
MEM_A_DQ<27>	AW36	SA_DQ27	
MEM_A_DQ<28>	AW41	SA_DQ28	
MEM_A_DQ<29>	AY41	SA_DQ29	
MEM_A_DQ<30>	AV38	SA_DQ30	
MEM_A_DQ<31>	AT38	SA_DQ31	
MEM_A_DQ<32>	AV13	SA_DQ32	
MEM_A_DQ<33>	AT13	SA_DQ33	
MEM_A_DQ<34>	AW11	SA_DQ34	
MEM_A_DQ<35>	AV11	SA_DQ35	
MEM_A_DQ<36>	AU15	SA_DQ36	
MEM_A_DQ<37>	AT11	SA_DQ37	
MEM_A_DQ<38>	BA13	SA_DQ38	
MEM_A_DQ<39>	BA11	SA_DQ39	
MEM_A_DQ<40>	BE10	SA_DQ40	
MEM_A_DQ<41>	BD10	SA_DQ41	
MEM_A_DQ<42>	BD8	SA_DQ42	
MEM_A_DQ<43>	AY9	SA_DQ43	
MEM_A_DQ<44>	BG10	SA_DQ44	
MEM_A_DQ<45>	AW9	SA_DQ45	
MEM_A_DQ<46>	BD7	SA_DQ46	
MEM_A_DQ<47>	BB9	SA_DQ47	
MEM_A_DQ<48>	BB5	SA_DQ48	
MEM_A_DQ<49>	AY7	SA_DQ49	
MEM_A_DQ<50>	AT5	SA_DQ50	
MEM_A_DQ<51>	AT7	SA_DQ51	
MEM_A_DQ<52>	AY6	SA_DQ52	
MEM_A_DQ<53>	BB7	SA_DQ53	
MEM_A_DQ<54>	AR5	SA_DQ54	
MEM_A_DQ<55>	AR8	SA_DQ55	
MEM_A_DQ<56>	AR9	SA_DQ56	
MEM_A_DQ<57>	AN3	SA_DQ57	
MEM_A_DQ<58>	AM8	SA_DQ58	
MEM_A_DQ<59>	AN10	SA_DQ59	
MEM_A_DQ<60>	AT9	SA_DQ60	
MEM_A_DQ<61>	AN9	SA_DQ61	
MEM_A_DQ<62>	AM9	SA_DQ62	
MEM_A_DQ<63>	AN11	SA_DQ63	

SA_BS0	BB19	MEM_A_BS<0>	OUT
SA_BS1	BK19	MEM_A_BS<1>	OUT
SA_BS2	BF29	MEM_A_BS<2>	OUT
SA_CAS*	BL17	MEM_A_CAS_L	OUT
SA_DM0	AT45	MEM_A_DM<0>	OUT
SA_DM1	BD44	MEM_A_DM<1>	OUT
SA_DM2	BD42	MEM_A_DM<2>	OUT
SA_DM3	AW38	MEM_A_DM<3>	OUT
SA_DM4	AW13	MEM_A_DM<4>	OUT
SA_DM5	BG8	MEM_A_DM<5>	OUT
SA_DM6	AY5	MEM_A_DM<6>	OUT
SA_DM7	AN6	MEM_A_DM<7>	OUT
SA_DQS0	AT46	MEM_A_DQS_P<0>	BI
SA_DQS1	BE48	MEM_A_DQS_P<1>	BI
SA_DQS2	BB43	MEM_A_DQS_P<2>	BI
SA_DQS3	BC37	MEM_A_DQS_P<3>	BI
SA_DQS4	BB16	MEM_A_DQS_P<4>	BI
SA_DQS5	BH6	MEM_A_DQS_P<5>	BI
SA_DQS6	BB2	MEM_A_DQS_P<6>	BI
SA_DQS7	AP3	MEM_A_DQS_P<7>	BI
SA_DQS0*	AT47	MEM_A_DQS_N<0>	BI
SA_DQS1*	BD47	MEM_A_DQS_N<1>	BI
SA_DQS2*	BC41	MEM_A_DQS_N<2>	BI
SA_DQS3*	BA37	MEM_A_DQS_N<3>	BI
SA_DQS4*	BA16	MEM_A_DQS_N<4>	BI
SA_DQS5*	BH7	MEM_A_DQS_N<5>	BI
SA_DQS6*	BC1	MEM_A_DQS_N<6>	BI
SA_DQS7*	AP2	MEM_A_DQS_N<7>	BI
SA_MA0	BJ19	MEM_A_A<0>	OUT
SA_MA1	BD20	MEM_A_A<1>	OUT
SA_MA2	BK27	MEM_A_A<2>	OUT
SA_MA3	BH28	MEM_A_A<3>	OUT
SA_MA4	BL24	MEM_A_A<4>	OUT
SA_MA5	BK28	MEM_A_A<5>	OUT
SA_MA6	BJ27	MEM_A_A<6>	OUT
SA_MA7	BJ25	MEM_A_A<7>	OUT
SA_MA8	BL28	MEM_A_A<8>	OUT
SA_MA9	BA28	MEM_A_A<9>	OUT
SA_MA10	BC19	MEM_A_A<10>	OUT
SA_MA11	BE28	MEM_A_A<11>	OUT
SA_MA12	BG30	MEM_A_A<12>	OUT
SA_MA13	BJ16	MEM_A_A<13>	OUT
SA_RAS*	BE18	MEM_A_RAS_L	OUT
SA_RCVEN*	AY20	TP_MEM_A_RCVEN_L	
SA_WE*	BA19	MEM_A_WE_L	OUT

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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	AP49	SB_DQ0	
MEM_B_DQ<1>	AR51	SB_DQ1	
MEM_B_DQ<2>	AW50	SB_DQ2	
MEM_B_DQ<3>	AW51	SB_DQ3	
MEM_B_DQ<4>	AN51	SB_DQ4	
MEM_B_DQ<5>	AN50	SB_DQ5	
MEM_B_DQ<6>	AV50	SB_DQ6	
MEM_B_DQ<7>	AV49	SB_DQ7	
MEM_B_DQ<8>	BA50	SB_DQ8	
MEM_B_DQ<9>	BB50	SB_DQ9	
MEM_B_DQ<10>	BA49	SB_DQ10	
MEM_B_DQ<11>	BE50	SB_DQ11	
MEM_B_DQ<12>	BA51	SB_DQ12	
MEM_B_DQ<13>	AY49	SB_DQ13	
MEM_B_DQ<14>	BF50	SB_DQ14	
MEM_B_DQ<15>	BF49	SB_DQ15	
MEM_B_DQ<16>	BJ50	SB_DQ16	
MEM_B_DQ<17>	BJ44	SB_DQ17	
MEM_B_DQ<18>	BJ43	SB_DQ18	
MEM_B_DQ<19>	BL43	SB_DQ19	
MEM_B_DQ<20>	BK47	SB_DQ20	
MEM_B_DQ<21>	BK49	SB_DQ21	
MEM_B_DQ<22>	BK43	SB_DQ22	
MEM_B_DQ<23>	BK42	SB_DQ23	
MEM_B_DQ<24>	BJ41	SB_DQ24	
MEM_B_DQ<25>	BL41	SB_DQ25	
MEM_B_DQ<26>	BJ37	SB_DQ26	
MEM_B_DQ<27>	BJ36	SB_DQ27	
MEM_B_DQ<28>	BK41	SB_DQ28	
MEM_B_DQ<29>	BJ40	SB_DQ29	
MEM_B_DQ<30>	BL35	SB_DQ30	
MEM_B_DQ<31>	BK37	SB_DQ31	
MEM_B_DQ<32>	BK13	SB_DQ32	
MEM_B_DQ<33>	BE11	SB_DQ33	
MEM_B_DQ<34>	BK11	SB_DQ34	
MEM_B_DQ<35>	BC11	SB_DQ35	
MEM_B_DQ<36>	BC13	SB_DQ36	
MEM_B_DQ<37>	BE12	SB_DQ37	
MEM_B_DQ<38>	BC12	SB_DQ38	
MEM_B_DQ<39>	BG12	SB_DQ39	
MEM_B_DQ<40>	BJ10	SB_DQ40	
MEM_B_DQ<41>	BL9	SB_DQ41	
MEM_B_DQ<42>	BK5	SB_DQ42	
MEM_B_DQ<43>	BL5	SB_DQ43	
MEM_B_DQ<44>	BK9	SB_DQ44	
MEM_B_DQ<45>	BK10	SB_DQ45	
MEM_B_DQ<46>	BJ8	SB_DQ46	
MEM_B_DQ<47>	BJ6	SB_DQ47	
MEM_B_DQ<48>	BF4	SB_DQ48	
MEM_B_DQ<49>	BH5	SB_DQ49	
MEM_B_DQ<50>	BG1	SB_DQ50	
MEM_B_DQ<51>	BC2	SB_DQ51	
MEM_B_DQ<52>	BK3	SB_DQ52	
MEM_B_DQ<53>	BE4	SB_DQ53	
MEM_B_DQ<54>	BD3	SB_DQ54	
MEM_B_DQ<55>	BJ2	SB_DQ55	
MEM_B_DQ<56>	BA3	SB_DQ56	
MEM_B_DQ<57>	BB3	SB_DQ57	
MEM_B_DQ<58>	AR1	SB_DQ58	
MEM_B_DQ<59>	AT3	SB_DQ59	
MEM_B_DQ<60>	AY2	SB_DQ60	
MEM_B_DQ<61>	AY3	SB_DQ61	
MEM_B_DQ<62>	AU2	SB_DQ62	
MEM_B_DQ<63>	AT2	SB_DQ63	

SB_BS0	AY17	MEM_B_BS<0>	OUT
SB_BS1	BG18	MEM_B_BS<1>	OUT
SB_BS2	BG36	MEM_B_BS<2>	OUT
SB_CAS*	BE17	MEM_B_CAS_L	OUT
SB_DM0	AR50	MEM_B_DM<0>	OUT
SB_DM1	BD49	MEM_B_DM<1>	OUT
SB_DM2	BK45	MEM_B_DM<2>	OUT
SB_DM3	BL39	MEM_B_DM<3>	OUT
SB_DM4	BH12	MEM_B_DM<4>	OUT
SB_DM5	BJ7	MEM_B_DM<5>	OUT
SB_DM6	BF3	MEM_B_DM<6>	OUT
SB_DM7	AW2	MEM_B_DM<7>	OUT
SB_DQS0	AT50	MEM_B_DQS_P<0>	BI
SB_DQS1	BD50	MEM_B_DQS_P<1>	BI
SB_DQS2	BK46	MEM_B_DQS_P<2>	BI
SB_DQS3	BK39	MEM_B_DQS_P<3>	BI
SB_DQS4	BJ12	MEM_B_DQS_P<4>	BI
SB_DQS5	BL7	MEM_B_DQS_P<5>	BI
SB_DQS6	BE2	MEM_B_DQS_P<6>	BI
SB_DQS7	AV2	MEM_B_DQS_P<7>	BI
SB_DQS0*	AU50	MEM_B_DQS_N<0>	BI
SB_DQS1*	BC50	MEM_B_DQS_N<1>	BI
SB_DQS2*	BL45	MEM_B_DQS_N<2>	BI
SB_DQS3*	BK38	MEM_B_DQS_N<3>	BI
SB_DQS4*	BK12	MEM_B_DQS_N<4>	BI
SB_DQS5*	BK7	MEM_B_DQS_N<5>	BI
SB_DQS6*	BF2	MEM_B_DQS_N<6>	BI
SB_DQS7*	AV3	MEM_B_DQS_N<7>	BI
SB_MA0	BC18	MEM_B_A<0>	OUT
SB_MA1	BG28	MEM_B_A<1>	OUT
SB_MA2	BG25	MEM_B_A<2>	OUT
SB_MA3	AW17	MEM_B_A<3>	OUT
SB_MA4	BF25	MEM_B_A<4>	OUT
SB_MA5	BE25	MEM_B_A<5>	OUT
SB_MA6	BA29	MEM_B_A<6>	OUT
SB_MA7	BC28	MEM_B_A<7>	OUT
SB_MA8	AY28	MEM_B_A<8>	OUT
SB_MA9	BD37	MEM_B_A<9>	OUT
SB_MA10	BG17	MEM_B_A<10>	OUT
SB_MA11	BE37	MEM_B_A<11>	OUT
SB_MA12	BA39	MEM_B_A<12>	OUT
SB_MA13	BG13	MEM_B_A<13>	OUT
SB_RAS*	AV16	MEM_B_RAS_L	OUT
SB_RCVEN*	AY18	TP_MEM_B_RCVEN_L	
SB_WE*	BC17	MEM_B_WE_L	OUT

NB DDR2 Interfaces

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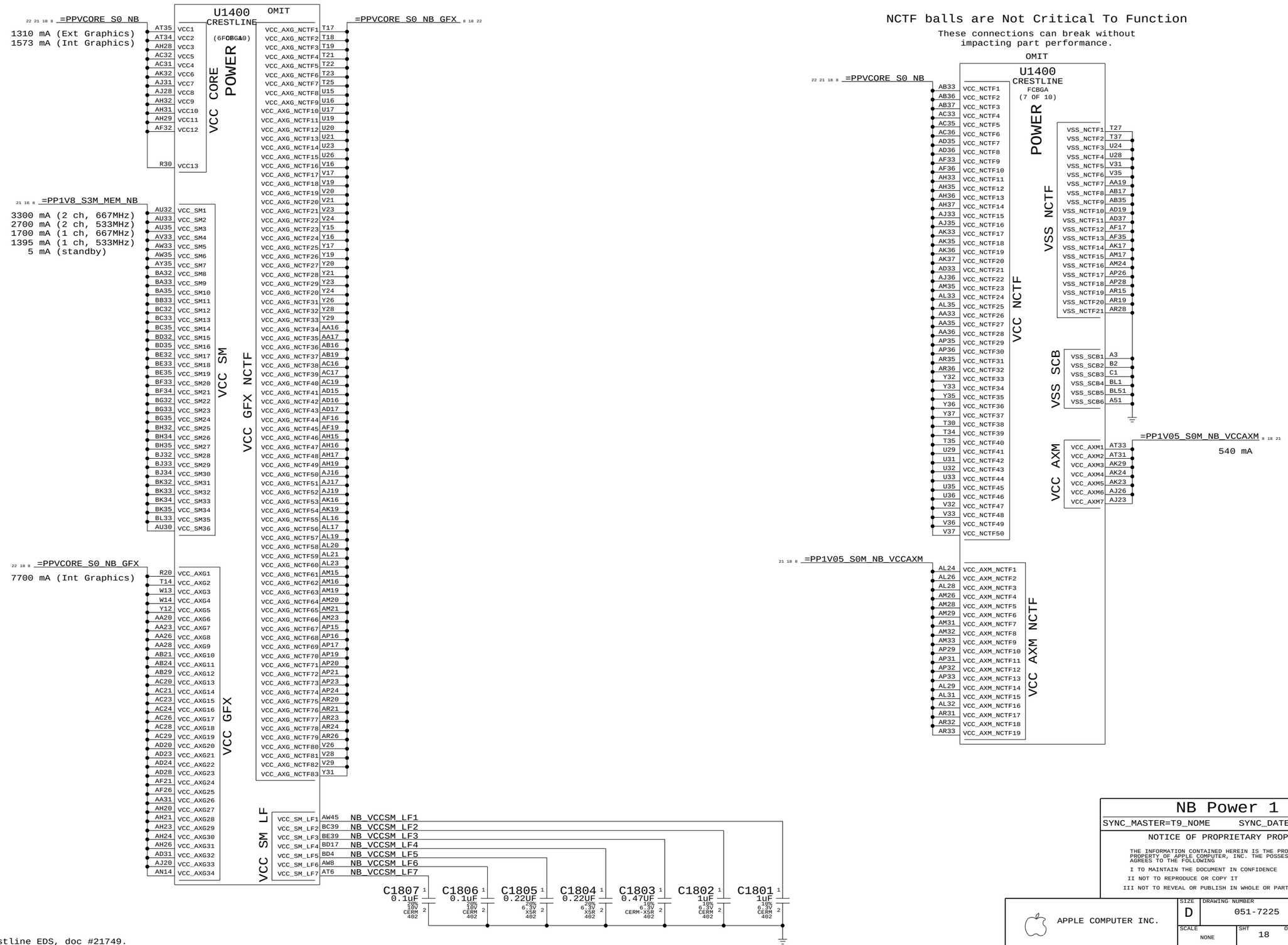

Current numbers from Crestline EDS, doc #21749.

NB Power 1

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CRESTLINE
FCBGA
(8 OF 10)

30 mA	22 =PP3V3_S0_NB_VCCSYNC	J32	VCC_SYNC	CRT POWER	
80 mA	22 PP3V3_S0_NB_VCCA_CRTDAC	A33	VCCA_CRT_DAC1		
		B33	VCCA_CRT_DAC2		
5 mA	22 PP3V3_S0_NB_VCCA_DAC_BG	A30	VCCA_DAC_BG		
	22 =GND_NB_VSSA_DAC_BG	B32	VSSA_DAC_BG		
100 mA	22 PP1V25_S0_NB_VCCA_DPLLA	B49	VCCA_DPLLA	PLL	
	22 PP1V25_S0_NB_VCCA_DPLLB	H49	VCCA_DPLLB		
50 mA	21 PP1V25_S0M_NB_VCCA_HPLL	AL2	VCCA_HPLL		
150 mA	21 PP1V25_S0M_NB_VCCA_MPLL	AM2	VCCA_MPLL		
	S0 or S3M is acceptable				
10 mA	22 19 PP1V8_S0_NB_VCCTXLVDS	A41	VCCA_LVDS	A LVDS	
	22 =GND_NB_VSSA_LVDS	B41	VSSA_LVDS		
0.4 mA	21 8 =PP3V3_S0_NB_VCCA_PEG_BG	K50	VCCA_PEG_BG	A PEG	
	21 =GND_NB_VSSA_PEG_BG	K49	VSSA_PEG_BG		
100 mA	21 PP1V25_S0_NB_PEGPLL	U51	VCCA_PEG_PLL		
640 mA (667MHz DDR) 550 mA (533MHz DDR)	21 PP1V25_S0M_NB_VCCA_SM	AW18	VCCA_SM1	A SM	
		AV19	VCCA_SM2		
		AU19	VCCA_SM3		
		AU18	VCCA_SM4		
		AU17	VCCA_SM5		
		AT22	VCCA_SM7		
		AT21	VCCA_SM8		
		AT19	VCCA_SM9		
		AT18	VCCA_SM10		
		AT17	VCCA_SM11		
		AR17	VCCA_SM_NCTF1		
		AR16	VCCA_SM_NCTF2		
35 mA	21 PP1V25_S0M_NB_VCCA_SM_CK	BC29	VCCA_SM_CK1	A CK	
		BB29	VCCA_SM_CK2		
40 mA	22 PP3V3_S0_NB_VCCA_TVDACC	C25	VCCA_TVA_DAC1	CRT	
		B25	VCCA_TVA_DAC2		
40 mA	22 PP3V3_S0_NB_VCCA_TVDACB	C27	VCCA_TVB_DAC1		
		B27	VCCA_TVB_DAC2		
40 mA	22 PP3V3_S0_NB_VCCA_TVDACA	B28	VCCA_TVC_DAC1		
		A28	VCCA_TVC_DAC2		
60 mA	22 =PP1V5_S0_NB_VCCD_CRT	M32	VCCD_CRT	TV/CRT	
60 mA	22 PP1V5_S0_NB_VCCD_TVDAC	L29	VCCD_TVDAC		
5 mA	22 PP1V5_S0_NB_VCCD_QDAC	N28	VCCD_QDAC		
250 mA	21 =PP1V25_S0M_NB_VCCD_HPLL	AN2	VCCD_HPLL	D	
		U48	VCCD_PEG_PLL		
150 mA	22 =PP1V8_S0_NB_VCCD_LVDS	J41	VCCD_LVDS1	LVDS	
		H42	VCCD_LVDS2		

VTT	VTT1 U13	=PP1V25R1V05_S0_NB_VTT 8 21	TBD mA @ 1067MHz FSB (1.25V) 850 mA @ 800MHz FSB (1.05V) 770 mA @ 667MHz FSB (1.05V)
	VTT2 U12		
	VTT3 U11		
	VTT4 U9		
	VTT5 U8		
	VTT6 U7		
	VTT7 U5		
	VTT8 U3		
	VTT9 U2		
	VTT10 U1		
	VTT11 T13		
	VTT12 T11		
	VTT13 T10		
	VTT14 T9		
	VTT15 T7		
	VTT16 T6		
	VTT17 T5		
	VTT18 T3		
	VTT19 T2		
	VTT20 R3		
	VTT21 R2		
	VTT22 R1		
AXD	VCC_AXD1 AT23	PP1V25_S0M_NB_VCCAXD 16 21	515 mA
	VCC_AXD2 AU28		
	VCC_AXD3 AU24		
	VCC_AXD4 AT29		
	VCC_AXD5 AT25		
	VCC_AXD6 AT30		
	VCC_AXD_NCTF AR29		
AXF	VCC_AXF1 B23	PP1V25_S0_NB_VCCAXF 21	495 mA
	VCC_AXF2 B21		
	VCC_AXF3 A21		
	VCC_DMI AJ50	=PP1V25_S0_NB_VCCDMI 8 21	100 mA
SM CK	VCC_SM_CK1 BK24	PP1V8_S3M_NB_VCCSMCK 21	200 mA
	VCC_SM_CK2 BK23		
	VCC_SM_CK3 BJ24		
	VCC_SM_CK4 BJ23		
	VCC_TX_LVDS A43	S0 or S3M is acceptable PP1V8_S0_NB_VCCTXLVDS 19 22	100 mA
HV	VCC_HV1 C40	=PP3V3_S0_NB_VCCHV 8 16 21	100 mA
	VCC_HV2 B40		
PEG	VCC_PEG1 AD51	PP1V05_S0_NB_VCCPEG 15 21	1260 mA
	VCC_PEG2 W50		
	VCC_PEG3 W51		
	VCC_PEG4 V49		
	VCC_PEG5 V50		
DMI	VCC_RXR_DMI1 AH50	PP1V05_S0_NB_VCCRXRDMI 21	260 mA
	VCC_RXR_DMI2 AH51		
VTTLF	VTTLF1 A7	NB_VTTLF_CAP1	
	VTTLF2 F2	NB_VTTLF_CAP2	
	VTTLF3 AH1	NB_VTTLF_CAP3	

C1913 0.47UF 10% 6.3V CERM-X5R 402
C1912 0.47UF 10% 6.3V CERM-X5R 402
C1911 0.47UF 10% 6.3V CERM-X5R 402

Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE NONE SHT 19 OF 88

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE VSS303	T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

=NB_TDE_SENSE S1

NOTE: TDE = _P

=NB_TDE_FORCE S1

=NB_TDB_FORCE S1

NOTE: TDB = _N

=NB_TDB_SENSE S1

NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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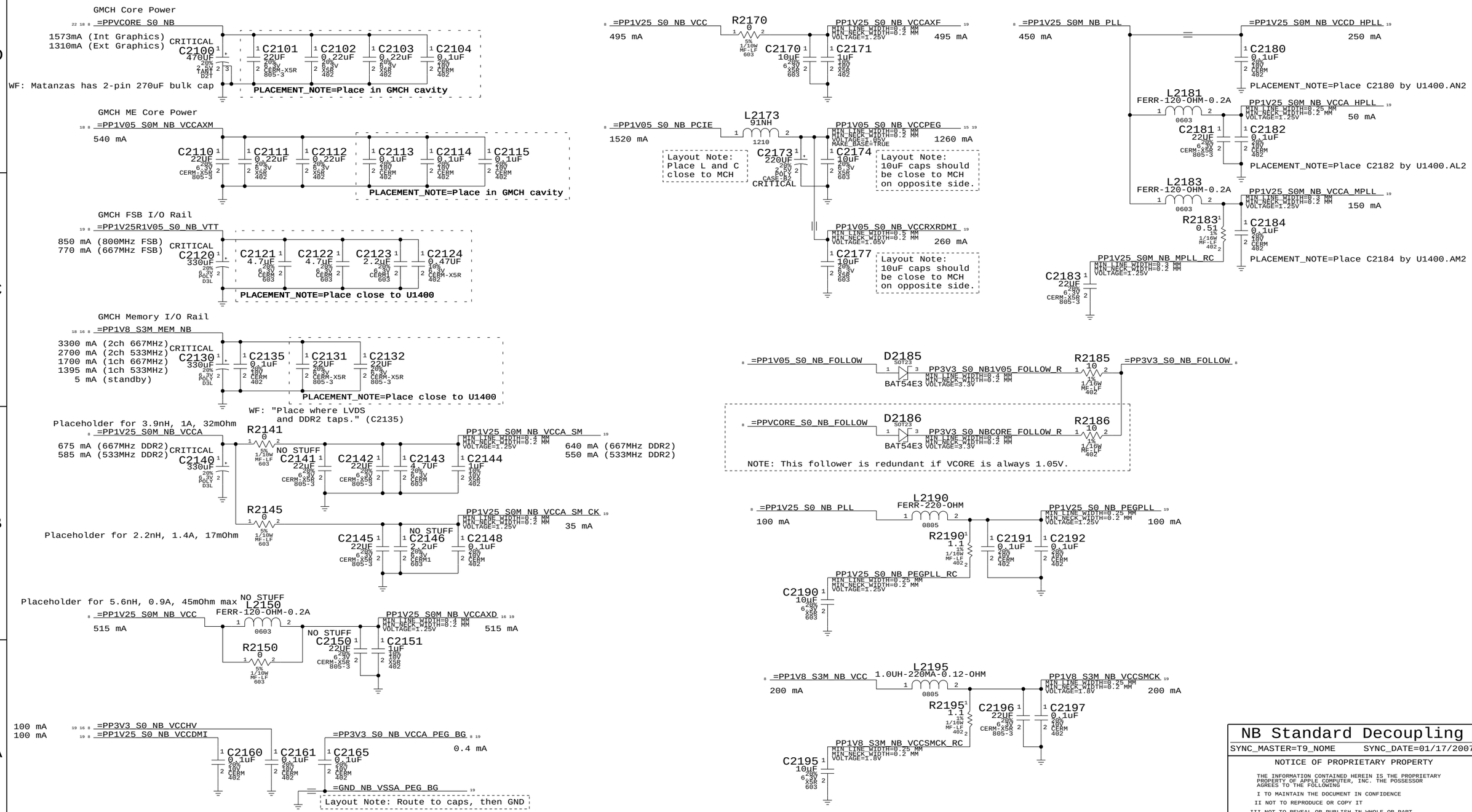
SCALE NONE SHT 20 OF 88



Current numbers from Crestline EDS, doc #21749.

NB Standard Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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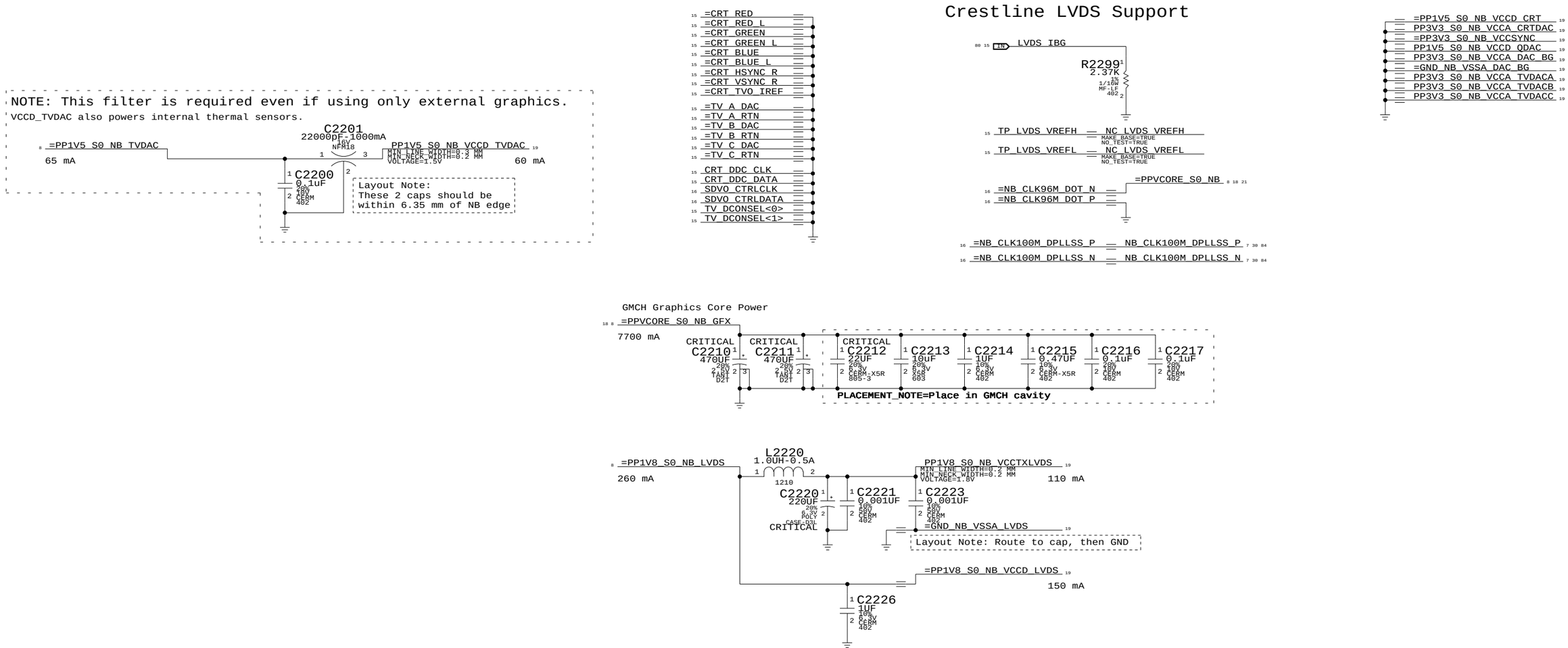

Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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SIZE	DRAWING NUMBER	REV.
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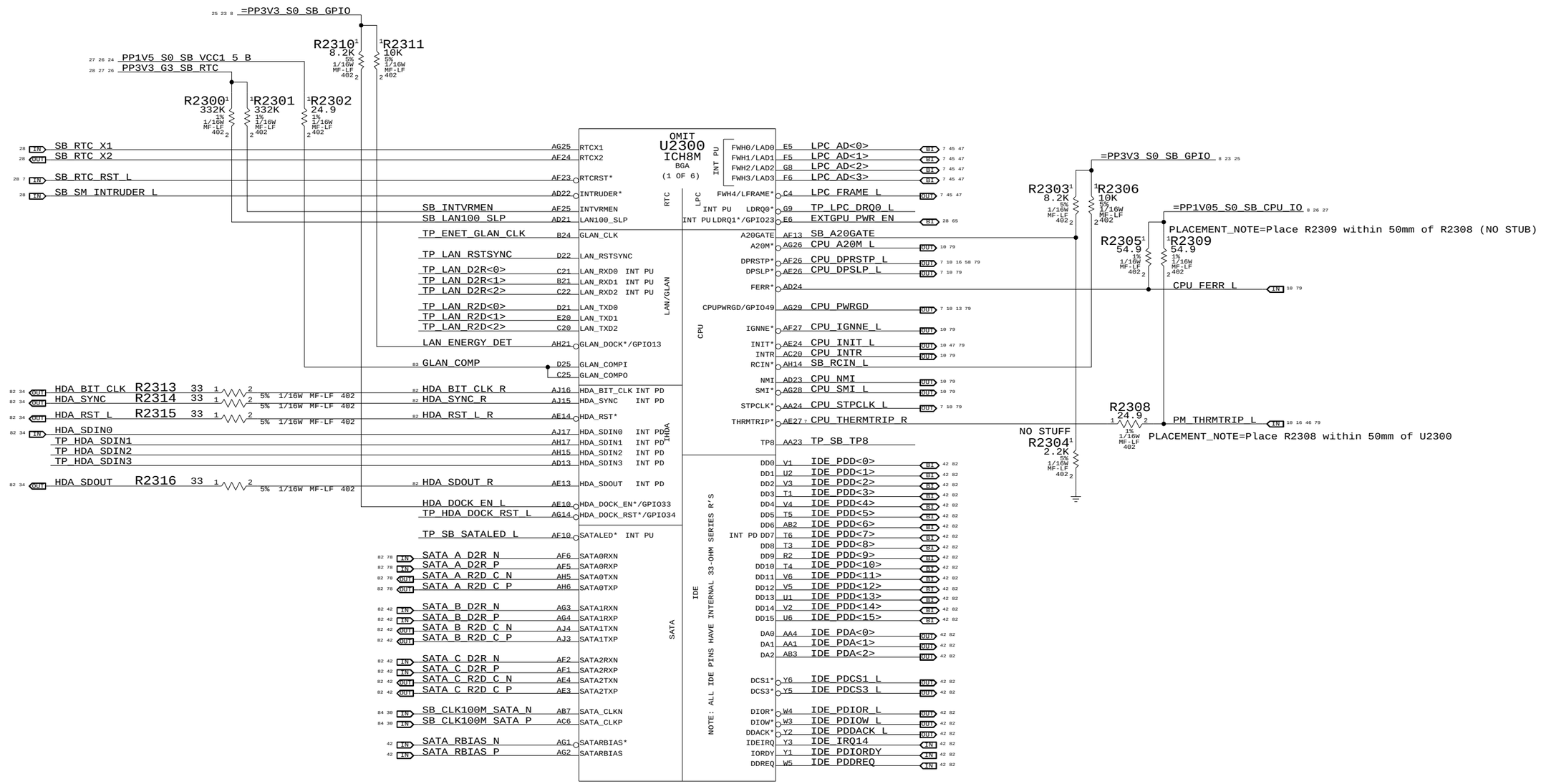
SCALE NONE	SHT 22 OF 88	



	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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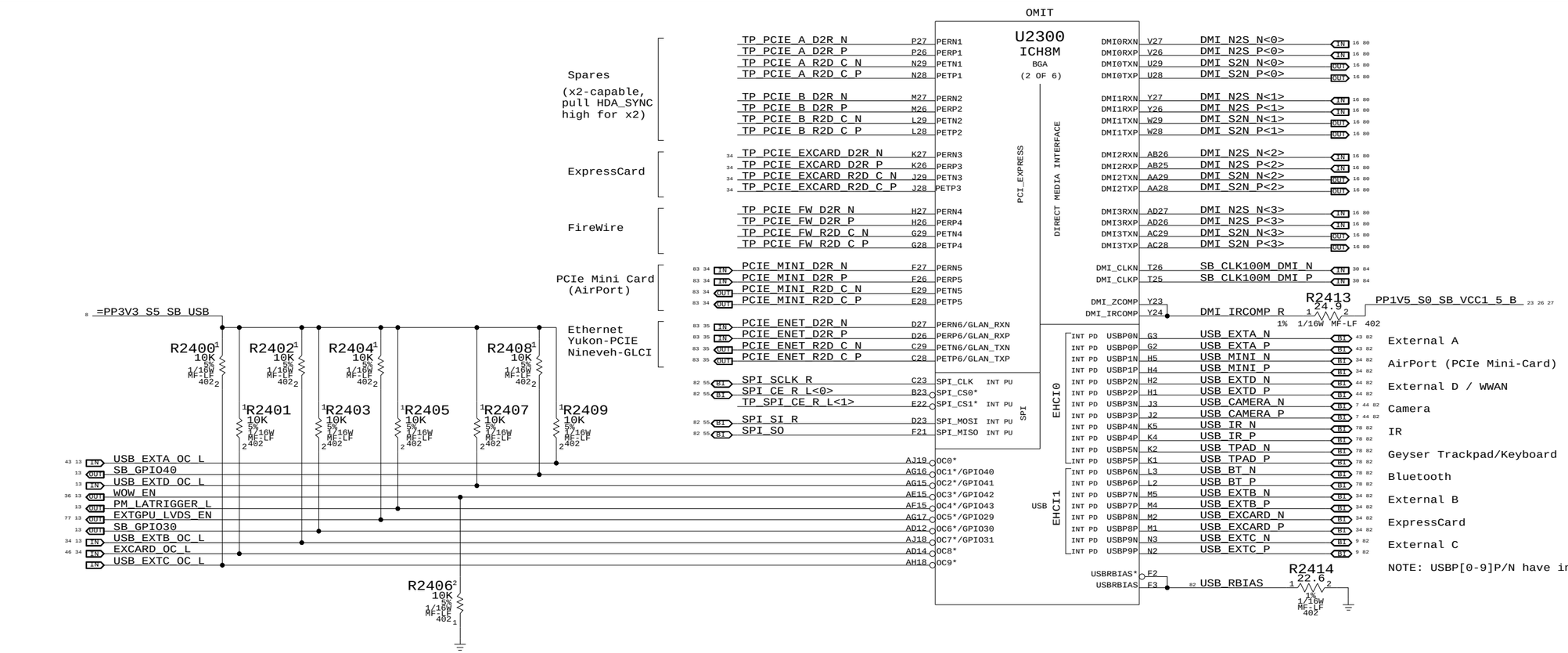

SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB PCI, PCIe, DMI, USB

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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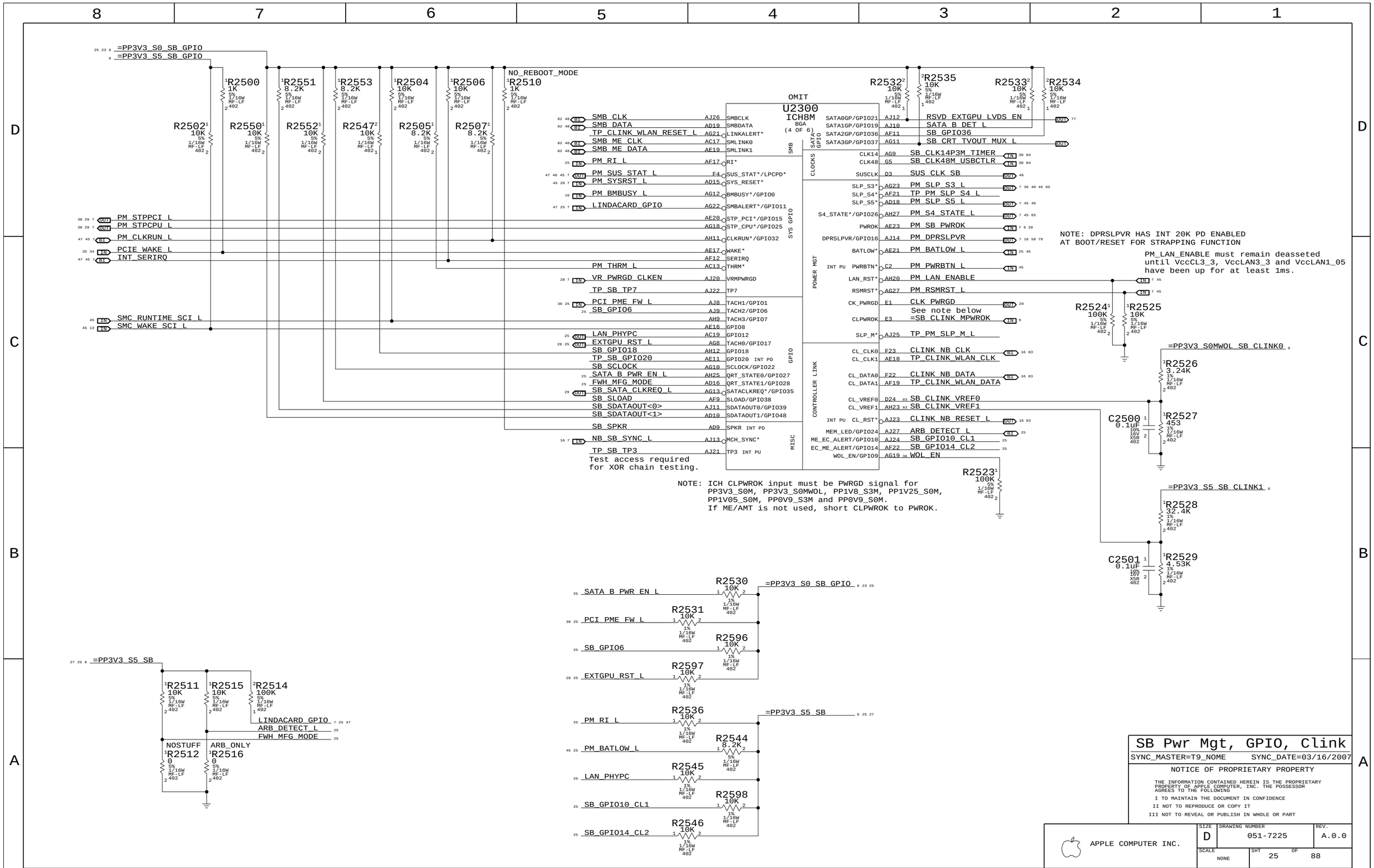
SCALE NONE	SHT 24 OF 88	



SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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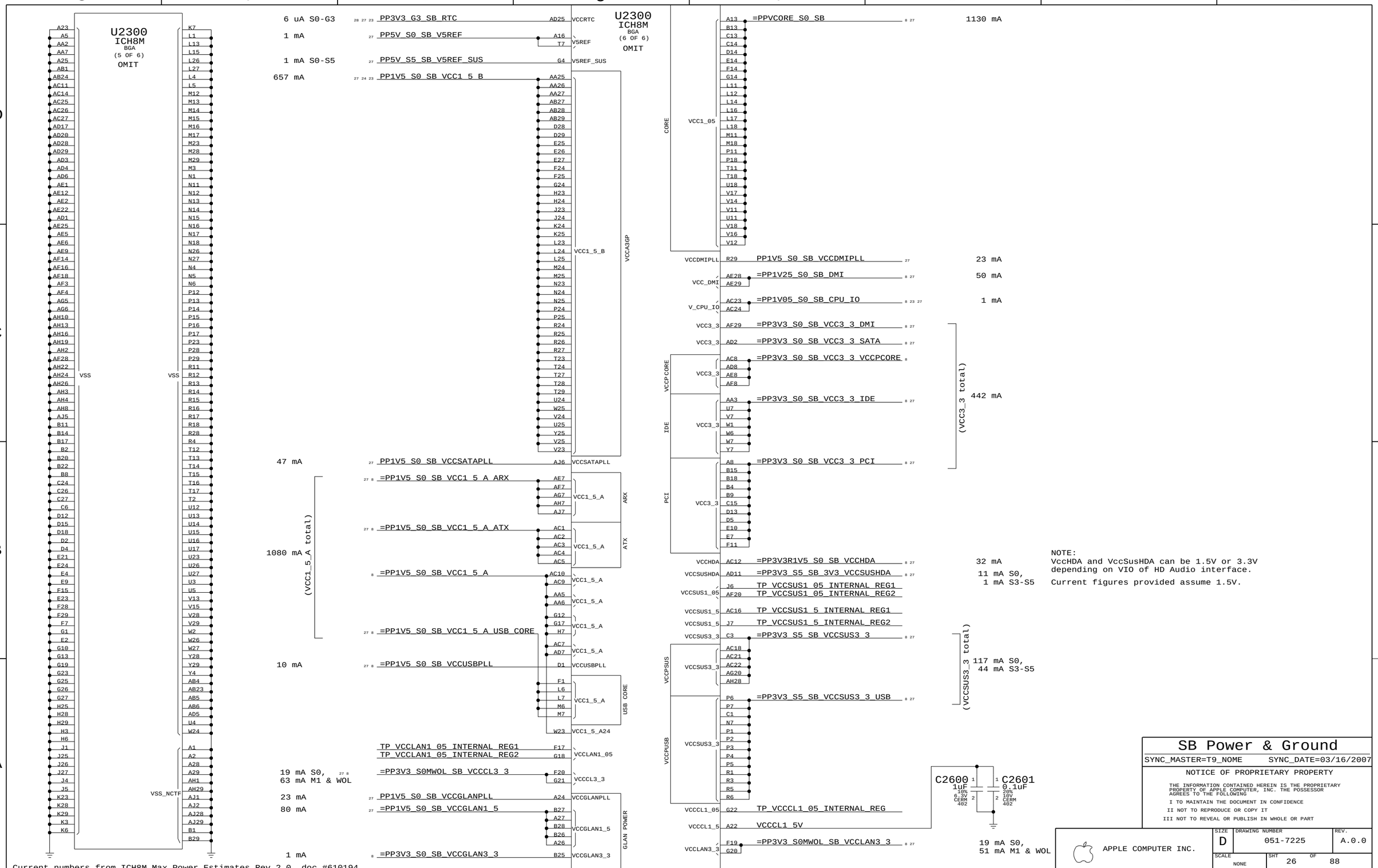
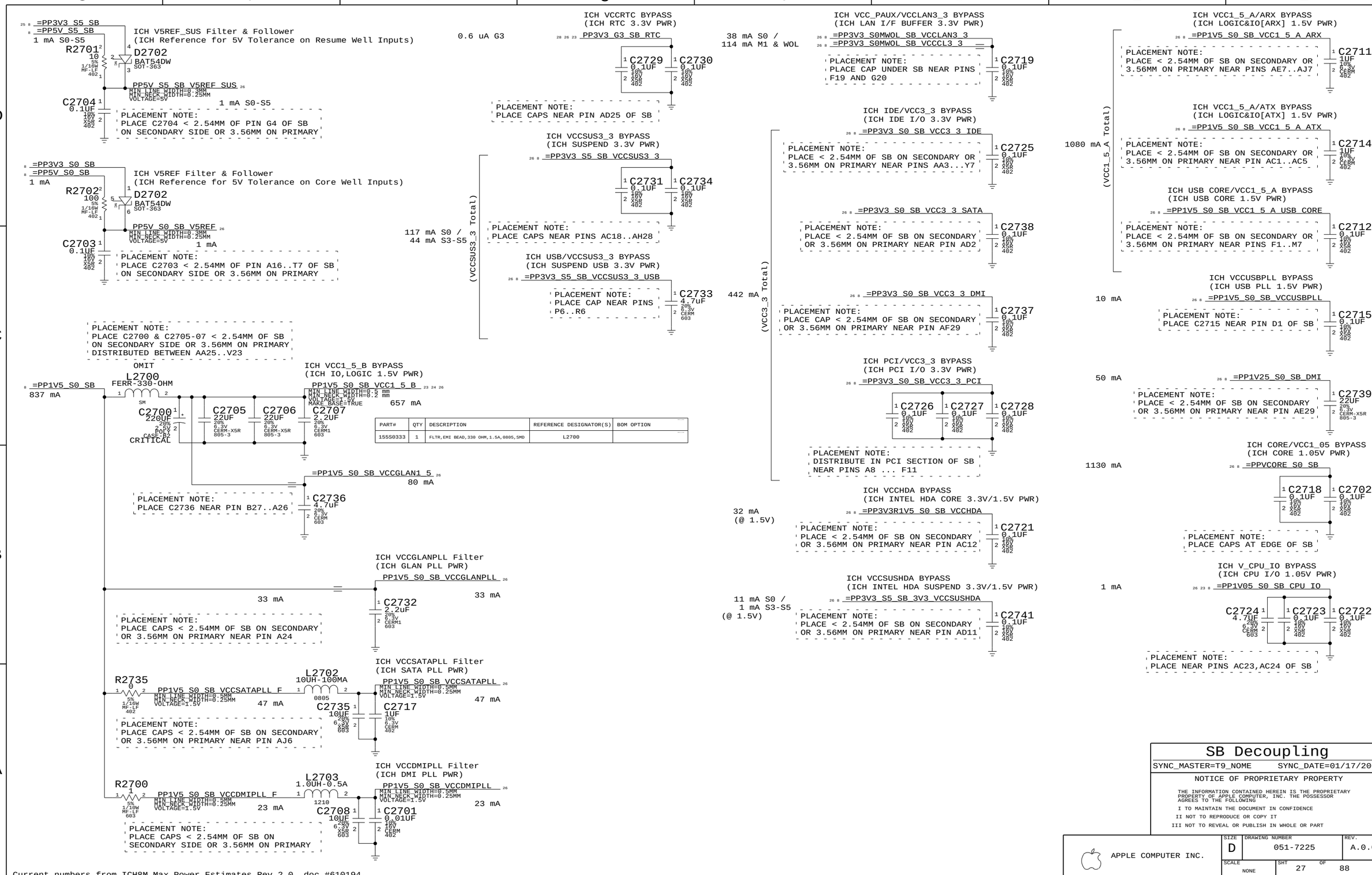
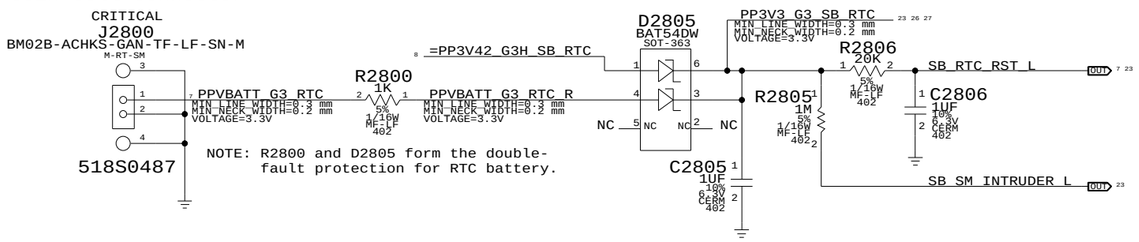


Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.



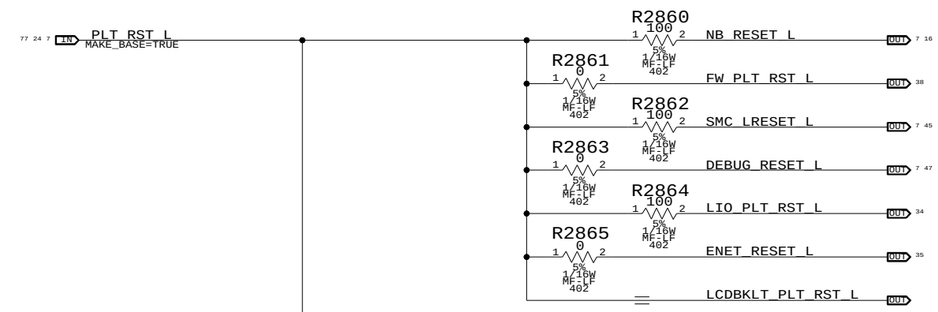
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0333	1	FLTR,EMI BEAD,330 OHM,1.5A,0805,SMD	L2700	

RTC Power Sources

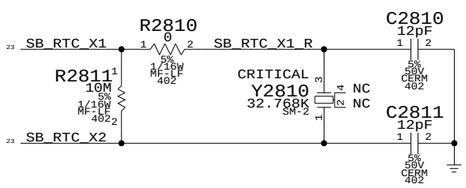


Platform Reset Connections

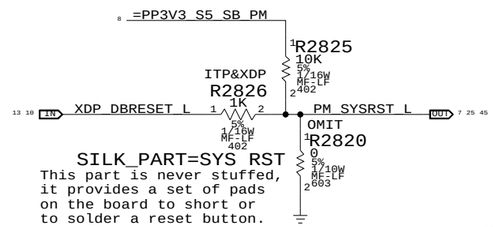
Unbuffered



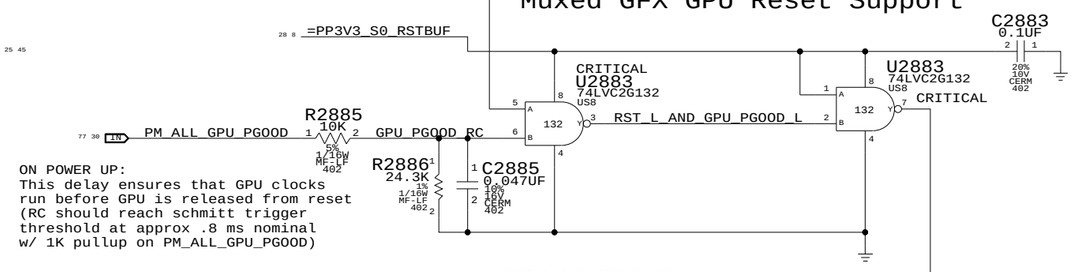
SB RTC Crystal



System Reset "Button"

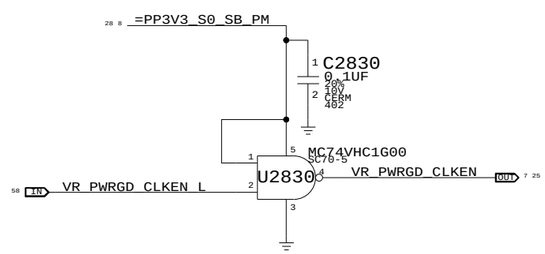


Muxed GFX GPU Reset Support

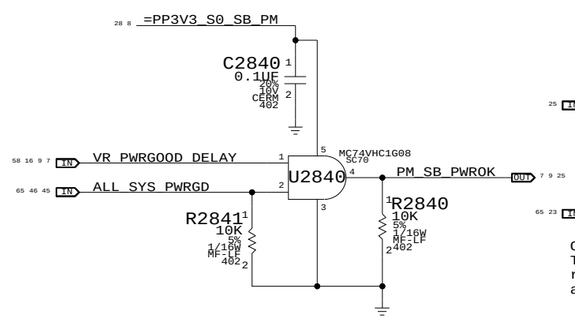


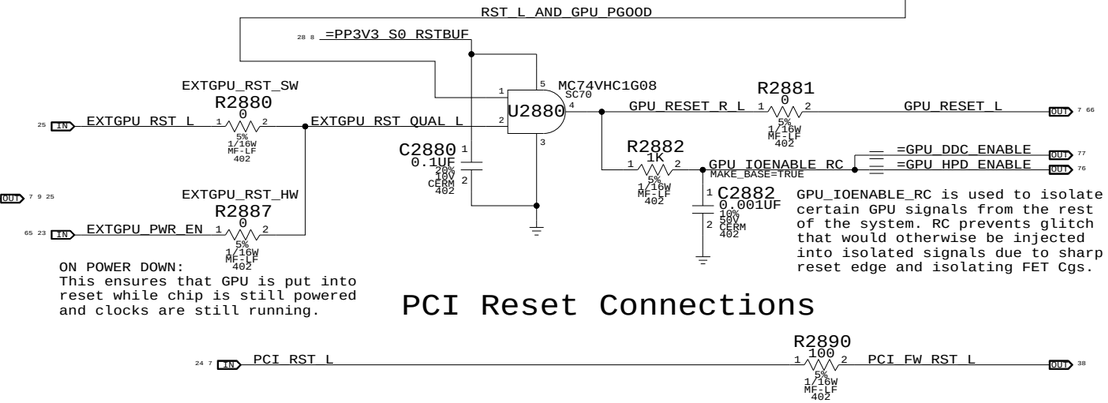
ON POWER UP:
This delay ensures that GPU clocks
run before GPU is released from reset
(RC should reach schmitt trigger
threshold at approx .8 ms nominal
w/ 1K pullup on PM_ALL_GPU_PGOOD)

VRMPWRGD Inverter



PWROK Circuit



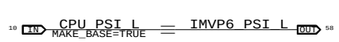


GPU_IOENABLE_RC is used to isolate
certain GPU signals from the rest
of the system. RC prevents glitch
that would otherwise be injected
into isolated signals due to sharp
reset edge and isolating FET Cgs.

ON POWER DOWN:
This ensures that GPU is put into
reset while chip is still powered
and clocks are still running.

PCI Reset Connections

CPU VCore ForcePSI



SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

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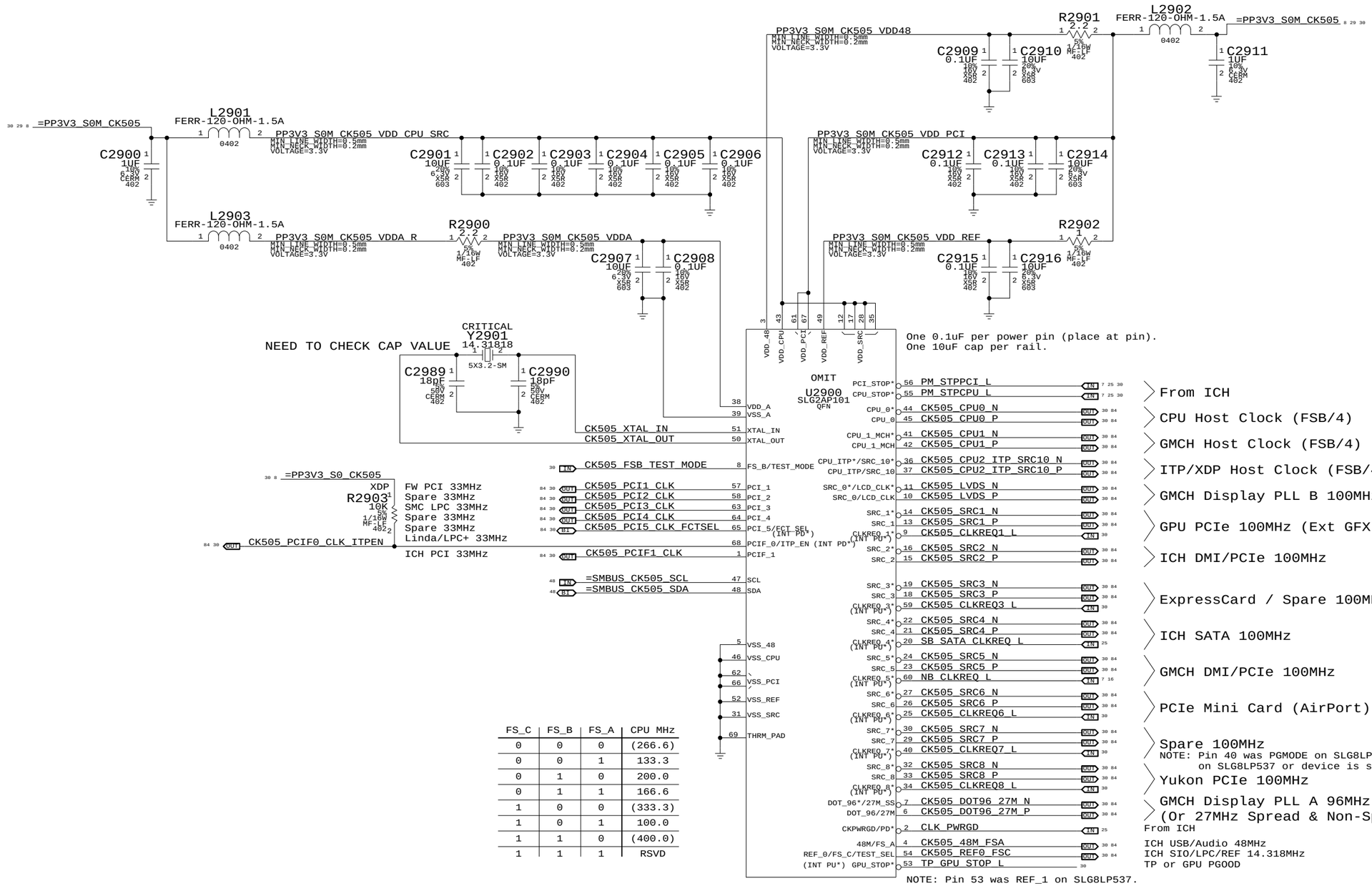
SCALE NONE	SHT 28 OF 88	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE NONE SHT 29 OF 88

CK505 Configuration Straps

FCT_SEL (GFX clock select)

=PP3V3_S0_CK505 — R3067[1] 10K 5% 1/16W MF-LF 402 — CK505_PCI5_CLK_FCTSEL

FS_A, FS_B, FS_C (Host clock freq select)

=PP1V25R1V05_S0_FSB_NB

NB_BSEL<0> — R3081 1K 5% 1/16W MF-LF 402 — CK505_FSA — R3082 0 5% 1/16W MF-LF 402 — CPU_BSEL<0>

(TO MCH FS_A) (FROM CPU FS_A)

NO STUFF R3080[1] 1K 5% 1/16W MF-LF 402

R3083[1] 1K 5% 1/16W MF-LF 402

R3033[2] 2.2K 5% 1/16W MF-LF 402

CK505_48M_FSA — R3032 33 5% 1/16W MF-LF 402 — SB_CLK48M_USBCTLR

(TO/FROM CK505) (TO ICH8M USB 48MHZ)

=PP1V25R1V05_S0_FSB_NB

NB_BSEL<1> — R3085 1K 5% 1/16W MF-LF 402 — NO STUFF — R3086 0 5% 1/16W MF-LF 402 — CPU_BSEL<1>

(TO MCH FS_B) (FROM CPU FS_B)

R3084[1] 1K 5% 1/16W MF-LF 402

R3087[1] 1K 5% 1/16W MF-LF 402

CK505_FSB_TEST_MODE

(TO CK505)

=PP1V25R1V05_S0_FSB_NB

NB_BSEL<2> — R3089 1K 5% 1/16W MF-LF 402 — CK505_FSC — R3090 0 5% 1/16W MF-LF 402 — CPU_BSEL<2>

(TO MCH FS_C) (FROM CPU FS_C)

NO STUFF R3088[1] 1K 5% 1/16W MF-LF 402

R3091[1] 1K 5% 1/16W MF-LF 402

R3035[2] 10K 5% 1/16W MF-LF 402

CK505_REF0_FSC — R3034 33 5% 1/16W MF-LF 402 — SB_CLK14P3M_TIMER

(TO/FROM CK505) (TO ICH8M 14.318MHZ)

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

CK505_CPU0_P — FSB_CLK_CPU_P (MAKE_BASE=TRUE)
CK505_CPU0_N — FSB_CLK_CPU_N (MAKE_BASE=TRUE)
(CPU HOST 167/200MHZ)

CK505_CPU1_P — FSB_CLK_NB_P (MAKE_BASE=TRUE)
CK505_CPU1_N — FSB_CLK_NB_N (MAKE_BASE=TRUE)
(GMCH HOST 167/200MHZ)

CK505_CPU2_ITP_SRC10_P — XDP_CLK_P (MAKE_BASE=TRUE)
CK505_CPU2_ITP_SRC10_N — XDP_CLK_N (MAKE_BASE=TRUE)
(ITP HOST 167/200MHZ)

CK505_LVDS_P — NB_CLK100M_DPLLSS_P (MAKE_BASE=TRUE)
CK505_LVDS_N — NB_CLK100M_DPLLSS_N (MAKE_BASE=TRUE)
(Int Gfx LVDS 100MHz)

CK505_SRC1_P — PEG_CLK100M_GPU_P (MAKE_BASE=TRUE)
CK505_SRC1_N — PEG_CLK100M_GPU_N (MAKE_BASE=TRUE)
(GPU PCIe 100MHz)

CK505_SRC2_P — SB_CLK100M_DMI_P (MAKE_BASE=TRUE)
CK505_SRC2_N — SB_CLK100M_DMI_N (MAKE_BASE=TRUE)
(ICH8M DMI 100MHZ)

CK505_SRC3_P — PCIE_CLK100M_EXCARD_P (MAKE_BASE=TRUE)
CK505_SRC3_N — PCIE_CLK100M_EXCARD_N (MAKE_BASE=TRUE)
(ExpressCard 100MHz)

CK505_SRC4_P — SB_CLK100M_SATA_P (MAKE_BASE=TRUE)
CK505_SRC4_N — SB_CLK100M_SATA_N (MAKE_BASE=TRUE)
(ICH8M SATA 100MHZ)

CK505_SRC5_P — NB_CLK100M_PCIE_P (MAKE_BASE=TRUE)
CK505_SRC5_N — NB_CLK100M_PCIE_N (MAKE_BASE=TRUE)
(GMCH PEG/DMI 100MHZ)

CK505_SRC6_P — PCIE_CLK100M_MINI_P (MAKE_BASE=TRUE)
CK505_SRC6_N — PCIE_CLK100M_MINI_N (MAKE_BASE=TRUE)
(WIRELESS PCIe MINI 100MHZ)

CK505_SRC7_P — TP_PCIE_CLK100M_SRC7P (MAKE_BASE=TRUE)
CK505_SRC7_N — TP_PCIE_CLK100M_SRC7N (MAKE_BASE=TRUE)
(FW 100MHz)

CK505_SRC8_P — PCIE_CLK100M_ENET_P (MAKE_BASE=TRUE)
CK505_SRC8_N — PCIE_CLK100M_ENET_N (MAKE_BASE=TRUE)
(ENET 100MHZ)

CK505_DOT96_27M_P — R3024 33 5% 1/16W MF-LF 402 — GPU_CLK27M
CK505_CLK27M (MAKE_BASE=TRUE)
(Ext GFX 27MHz)

CK505_DOT96_27M_N — R3025 33 5% 1/16W MF-LF 402 — GPU_CLK27M_SS
CK505_CLK27M_SS (MAKE_BASE=TRUE)
(Ext GFX Spread 27MHz)

CK505_PCIF0_CLK_ITPEN — R3026 33 5% 1/16W MF-LF 402 — PCI_CLK33M_LPCPLUS
(LINDA/LPC+ LPC 33MHZ)

CK505_PCIF1_CLK — R3027 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SB
(ICH8M PCI 33MHZ)

CK505_PCI1_CLK — R3028 33 5% 1/16W MF-LF 402 — PCI_CLK33M_FW
(FIREWIRE PCI 33MHZ)

CK505_PCI3_CLK — R3030 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SMC
(SMC PCI 33MHZ)

CLKREQ Controls

=PP3V3_S0M_CK505

PM_STPPCI_L — NO STUFF R3046 10K 5% 1/16W MF-LF 402

PM_STPCPU_L — NO STUFF R3047 10K 5% 1/16W MF-LF 402

Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

EXCARD_CLKREQ_L (MAKE_BASE=TRUE) — CK505_CLKREQ3_L
MINI_CLKREQ_L (MAKE_BASE=TRUE) — CK505_CLKREQ6_L
=ENET_CLKREQ_L — ENET_CLKREQ_L (MAKE_BASE=TRUE) — CK505_CLKREQ8_L
TP_CK505_CLKREQ7_L (MAKE_BASE=TRUE) — CK505_CLKREQ7_L

GPU Clock Gating

GPU_STOP_L (MAKE_BASE=TRUE) — TP_GPU_STOP_L
PEG_CLKREQ_L (MAKE_BASE=TRUE) — CK505_CLKREQ1_L

SLG2AP101 R3051[1] 0 5% 1/16W MF-LF 402 — SLG8LP537 Q3050 2N7002DW-X-F SOT-363 — PM_ALL_GPU_PGOOD

SLG8LP537 U3050 NC7SB3157P6X SC70

GPU_CLK27M — PM_ALL_GPU_PGOOD
SLG2AP101 R3050[1] 0 5% 1/16W MF-LF 402 — =PP3V3_S0_GPUCLKGATE
GPU_CLK27M_GATED
C3050 0.1UF 20% 10V CERM 402 — SLG8LP537

U3055 NC7SB3157P6X SC70

GPU_CLK27M_SS
SLG2AP101 R3055[1] 0 5% 1/16W MF-LF 402 — GPU_CLK27M_SS_GATED
C3055 0.1UF 20% 10V CERM 402 — GPU_SS_EXT

Unused Clocks

CK505_PCI2_CLK — TP_CK505_PCI2_CLK (MAKE_BASE=TRUE)
(Reserved for TPM PCI 33MHZ)

CK505_PCI4_CLK — TP_CK505_PCI4_CLK (MAKE_BASE=TRUE)
(Spare 33MHZ)

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

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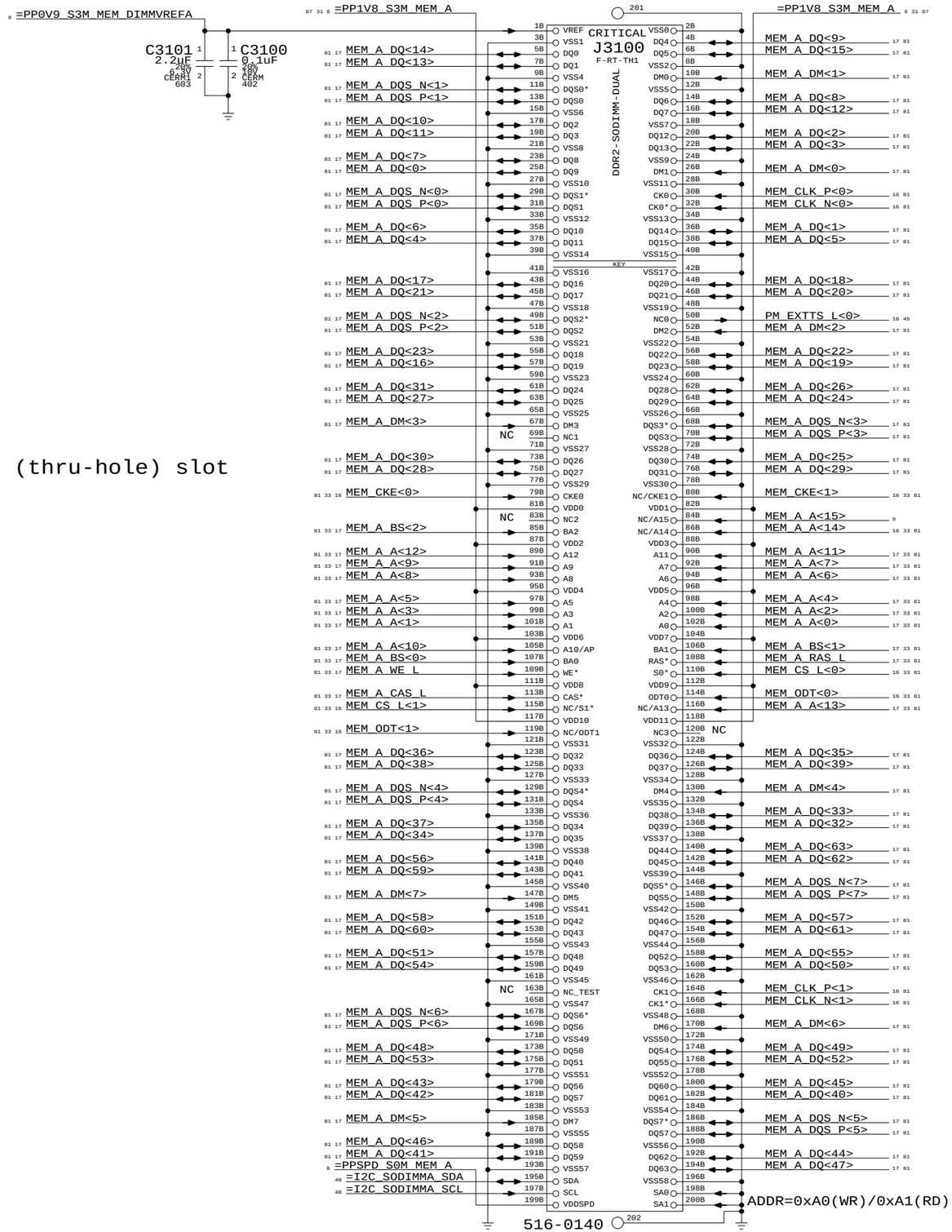
SCALE NONE — SHT 30 OF 88

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

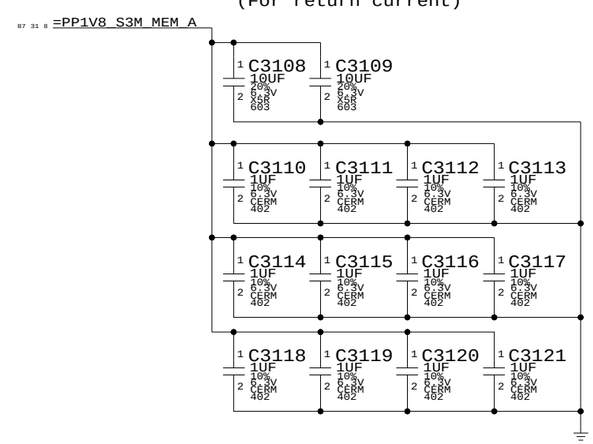
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



"Factory" (thru-hole) slot

DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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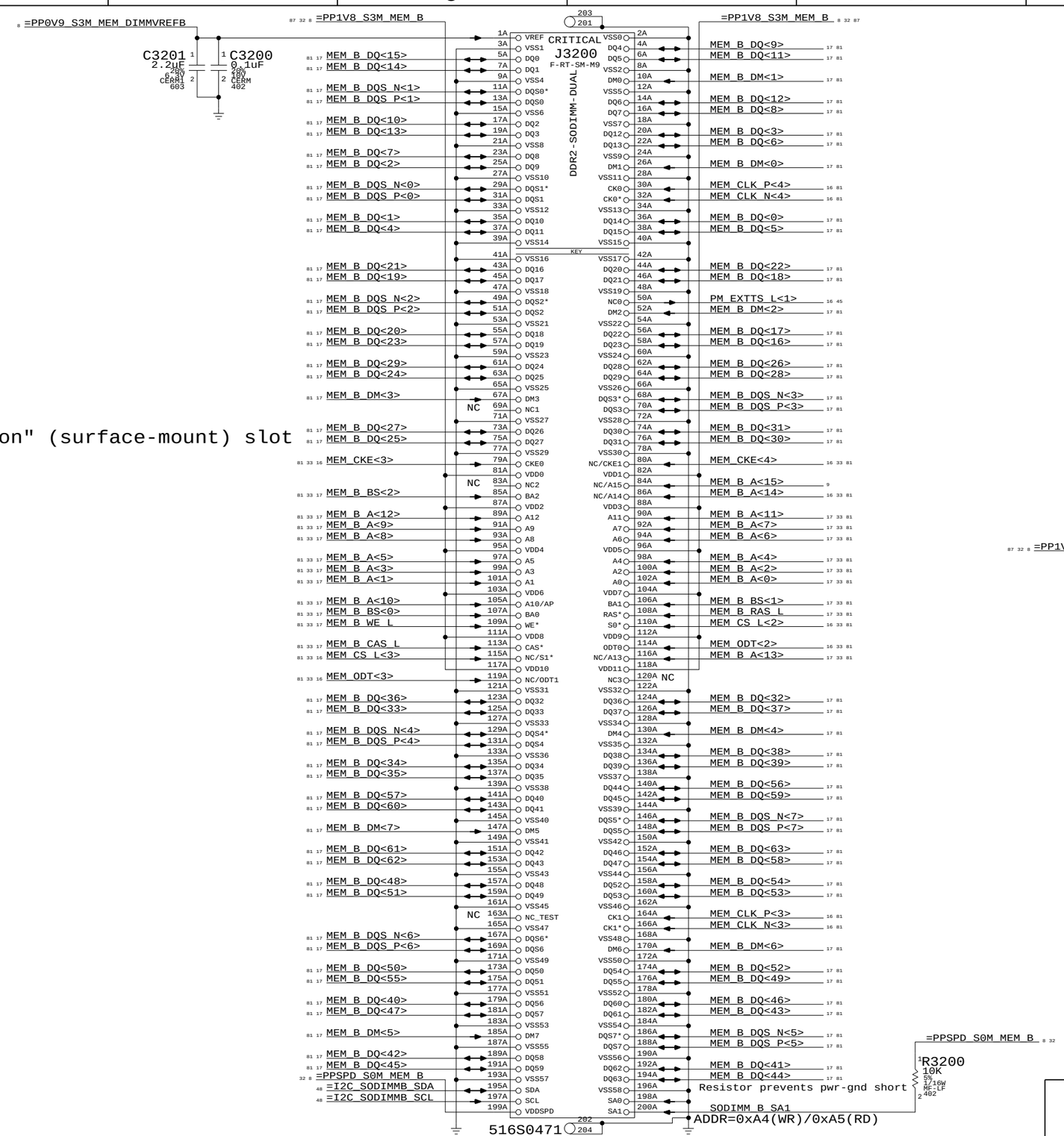
Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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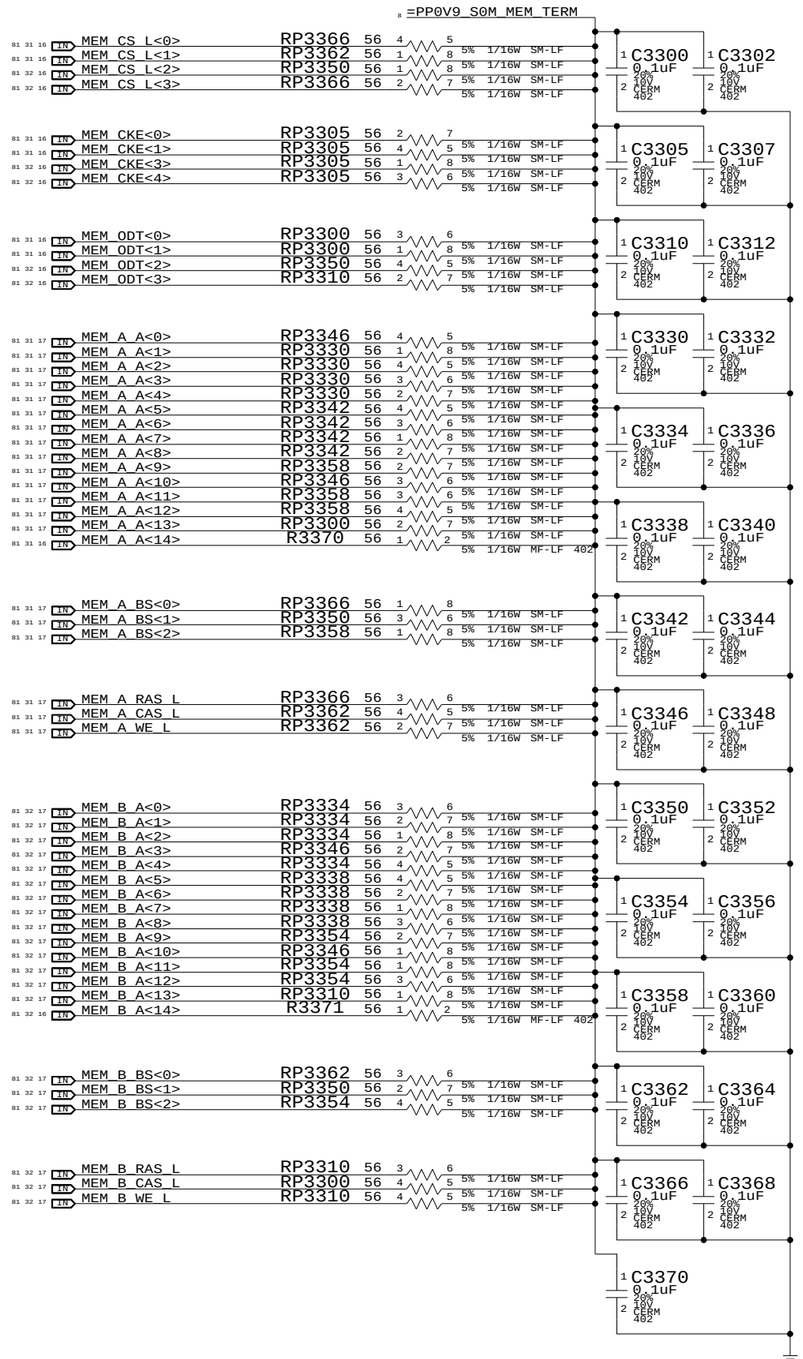
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

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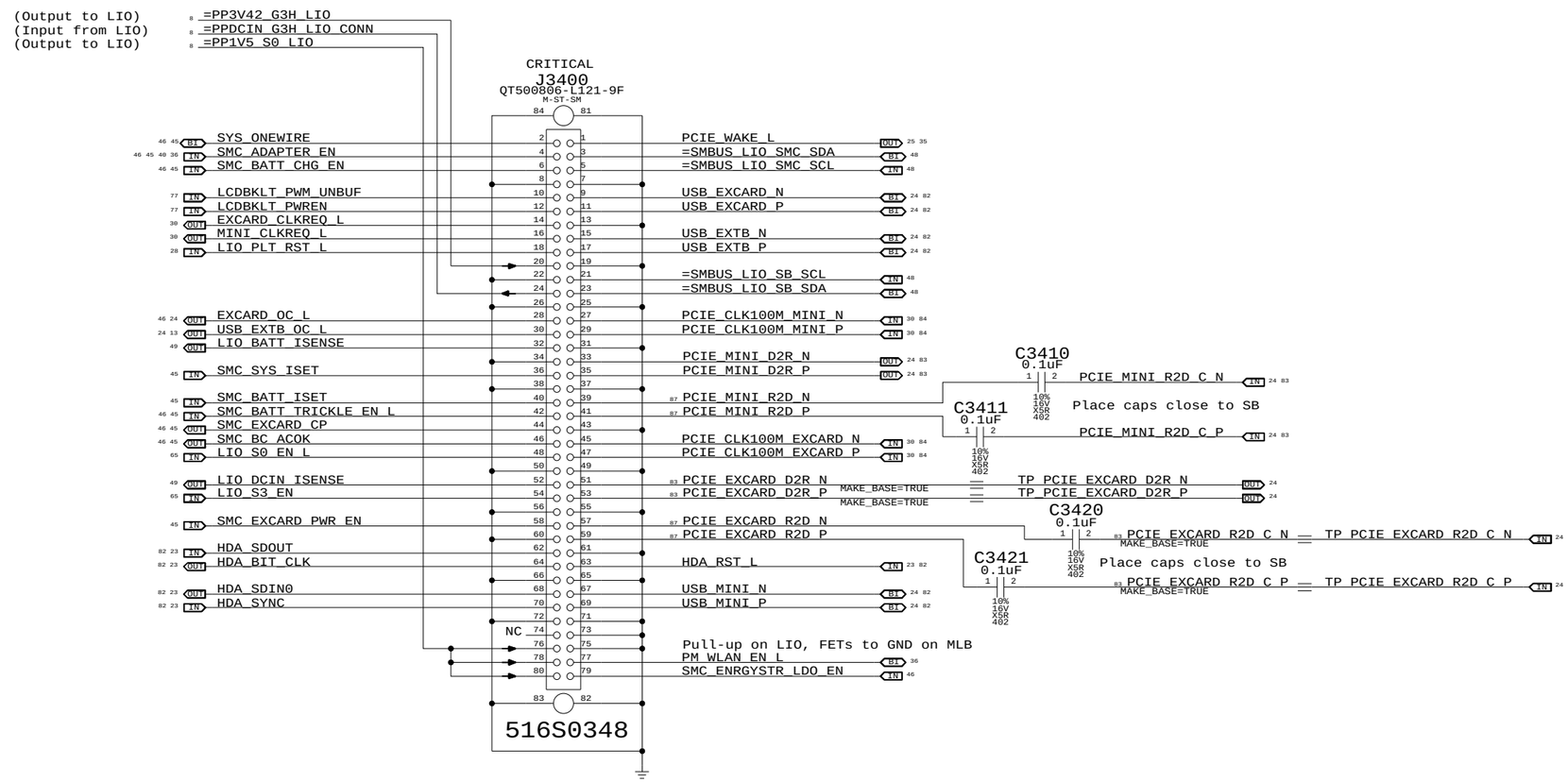
Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SCALE NONE

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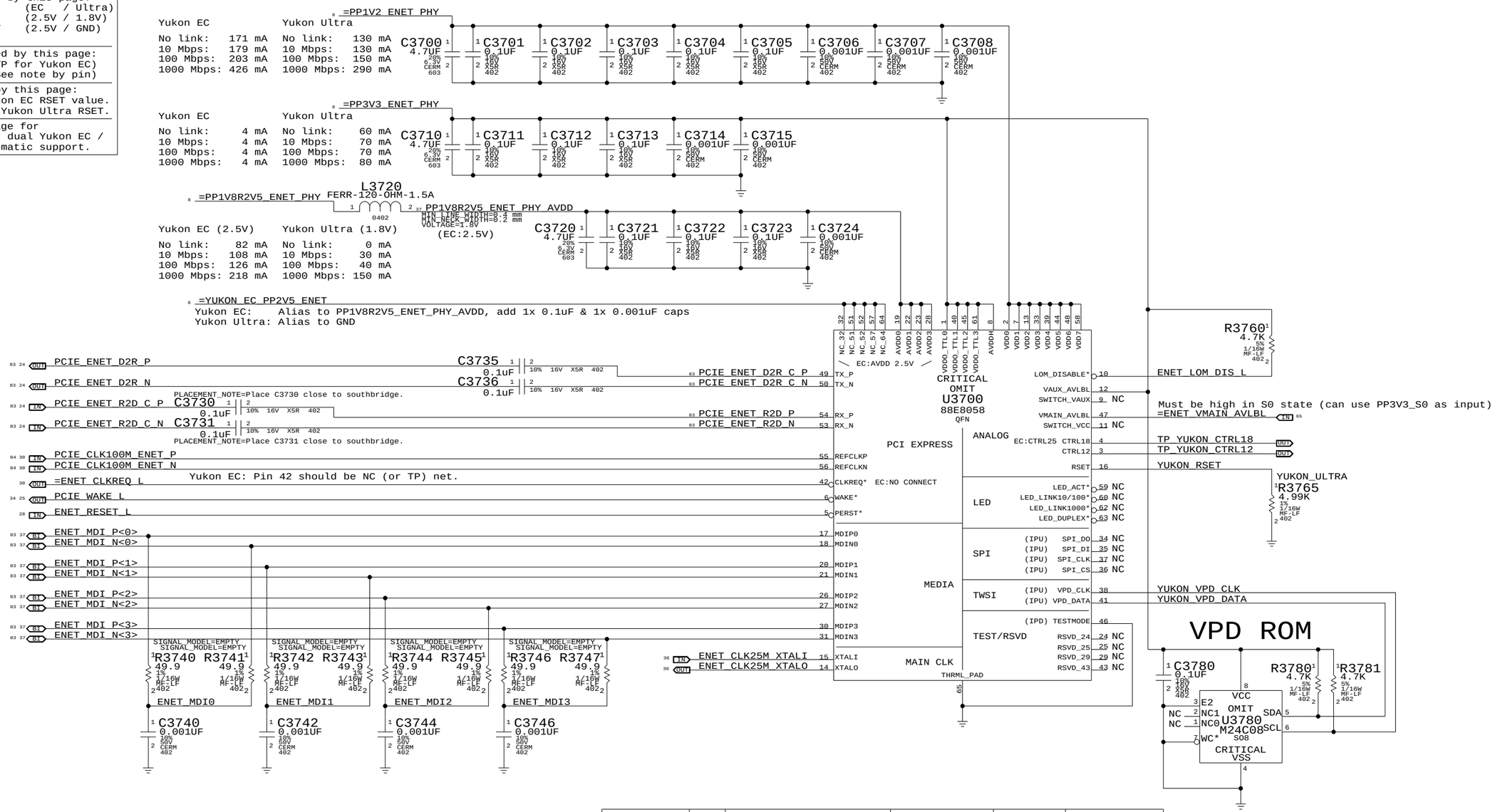
Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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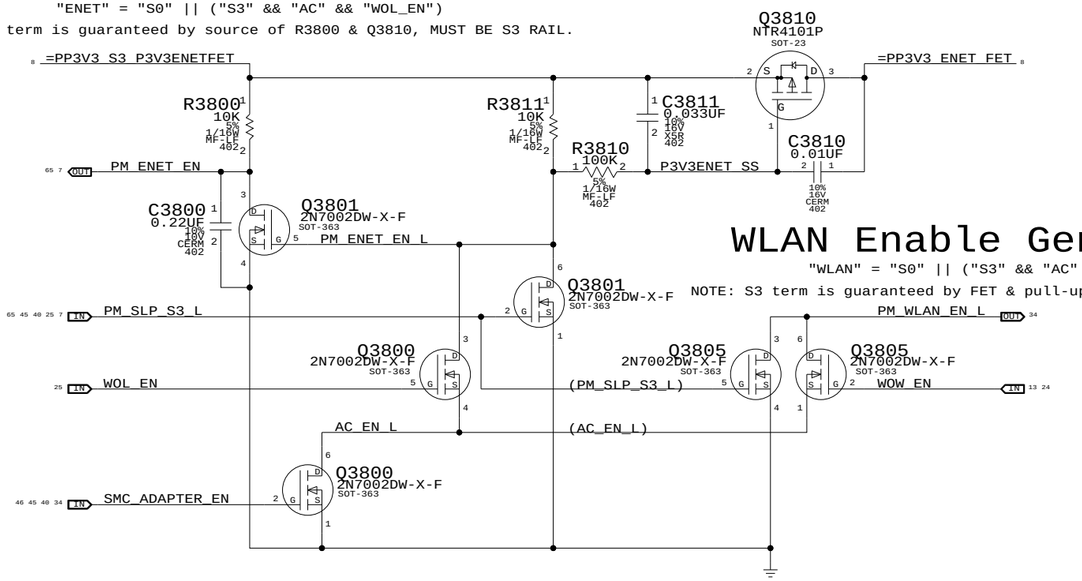
ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET



WLAN Enable Generation

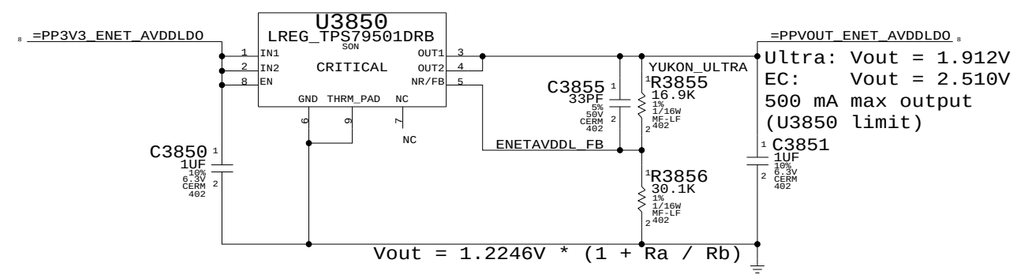
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

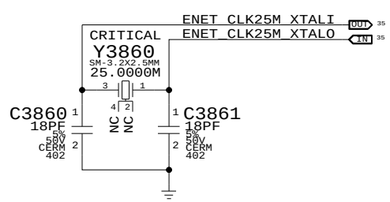
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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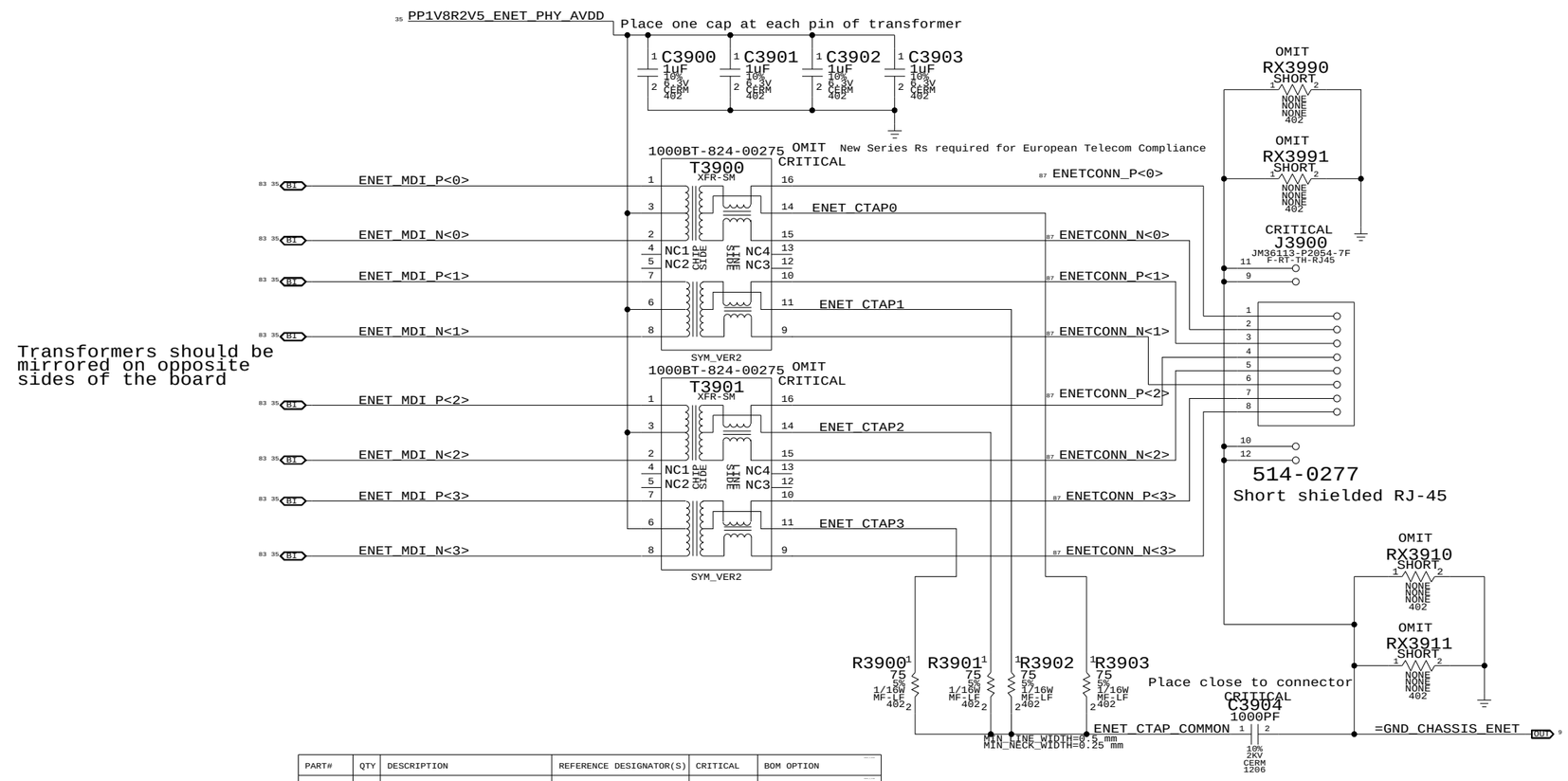
SCALE NONE

Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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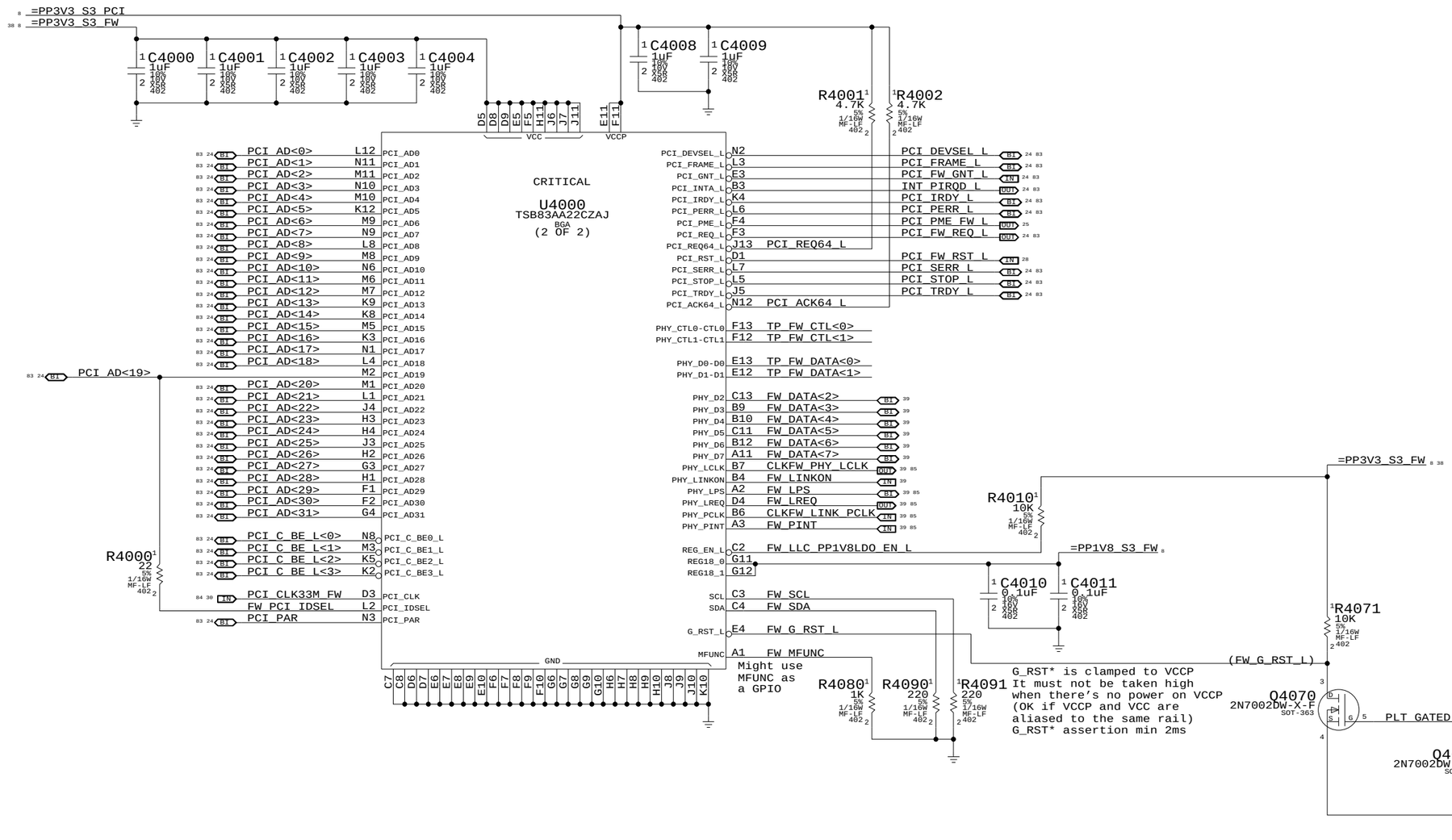
D	051-7225	A.0.0

SCALE NONE SHT 37 OF 88



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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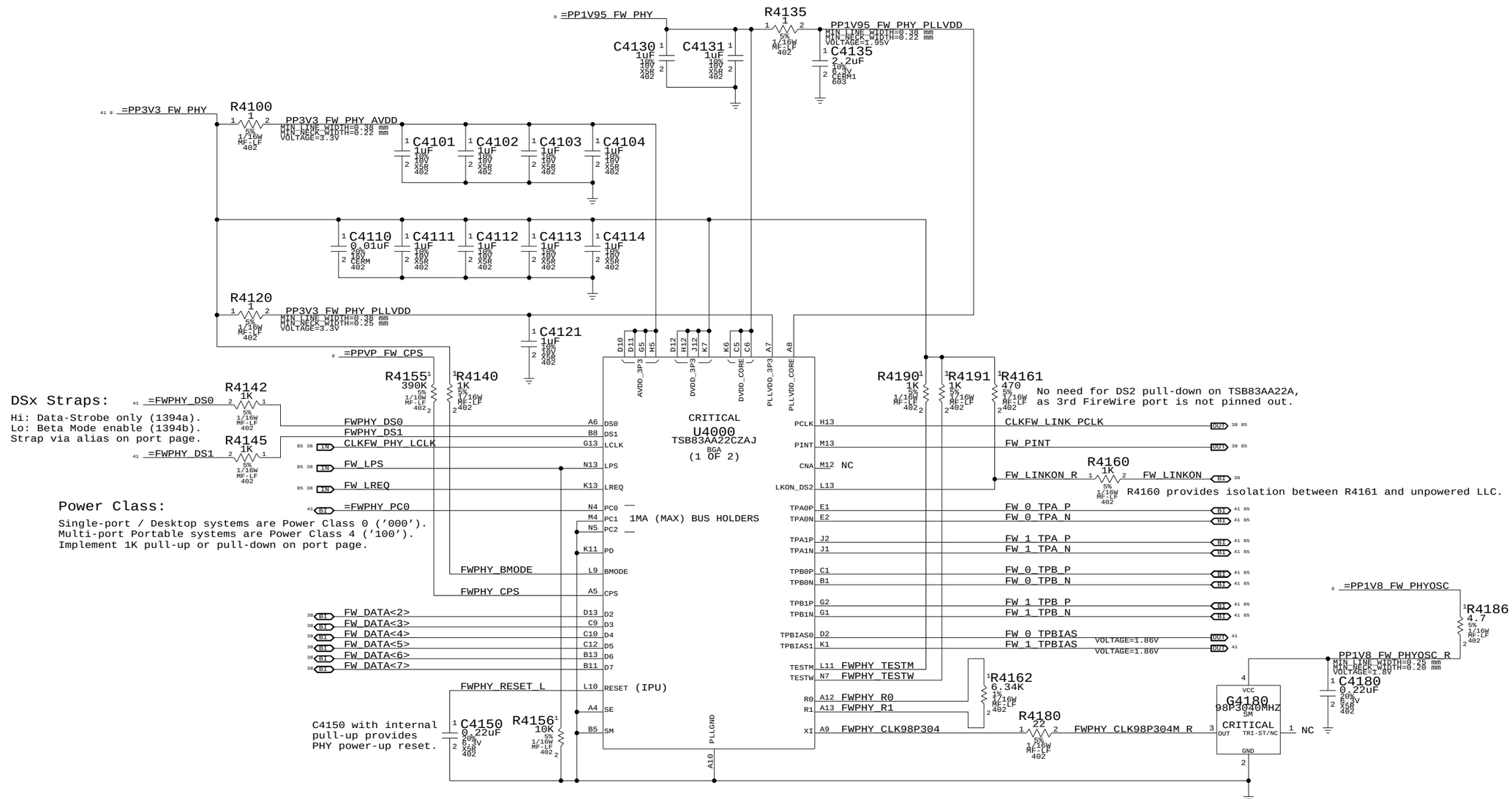
D	051-7225	A.0.0

SCALE NONE | SHT 38 OF 88



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 39 OF 88	

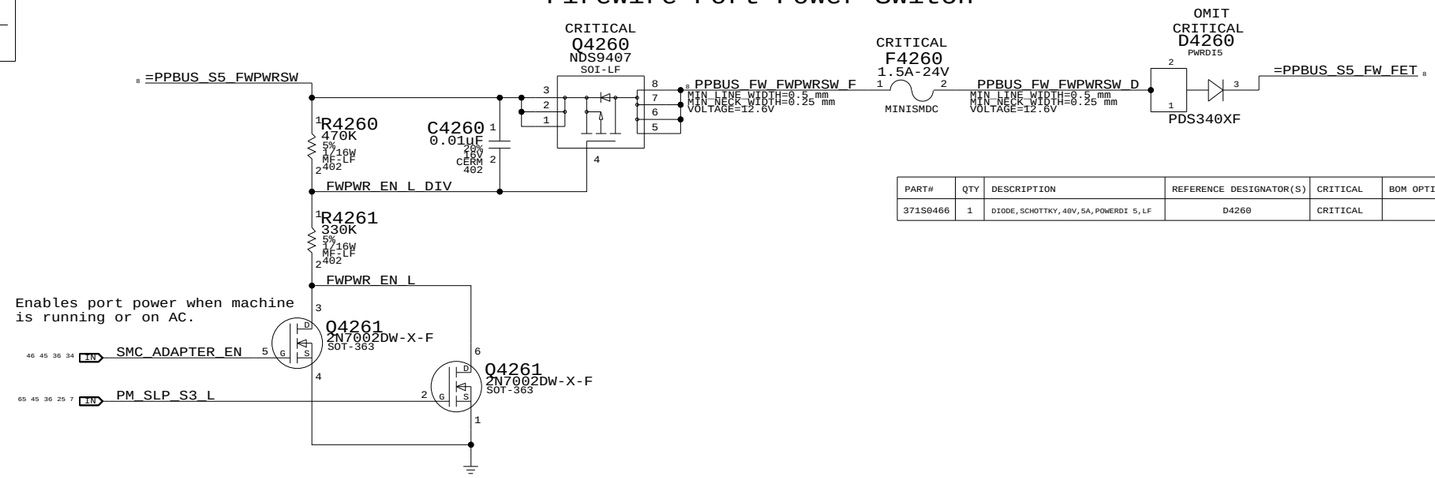
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

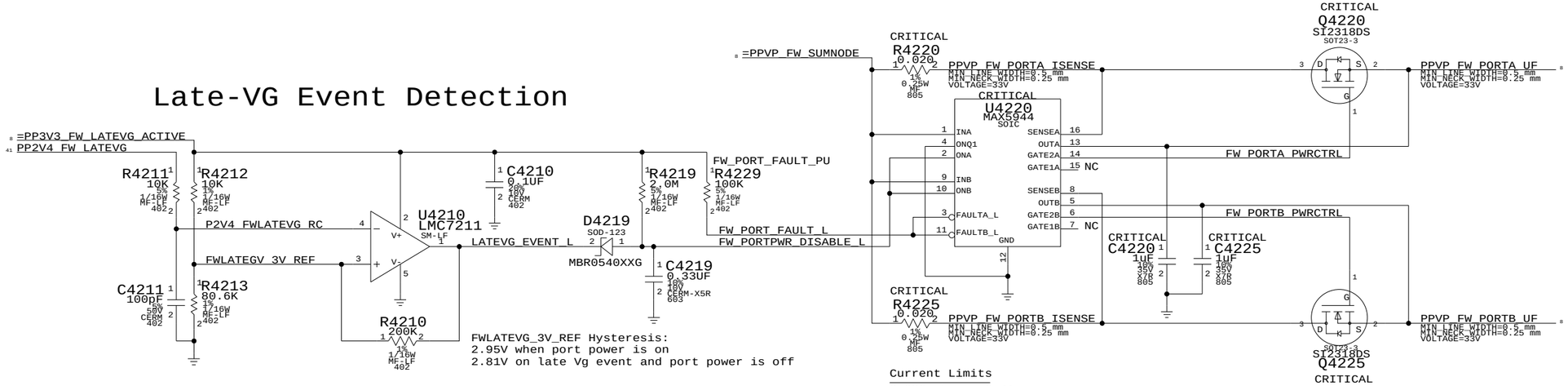
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
371S0466	1	DIODE,SCHOTTKY,40V,5A,POWERDI 5,LF	D4260	CRITICAL	

Current Limit/Active Late-VG Protection



Late-VG Event Detection

FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off

Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

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SCALE NONE SHT 40 OF 88

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

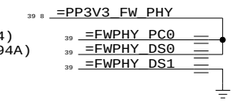
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

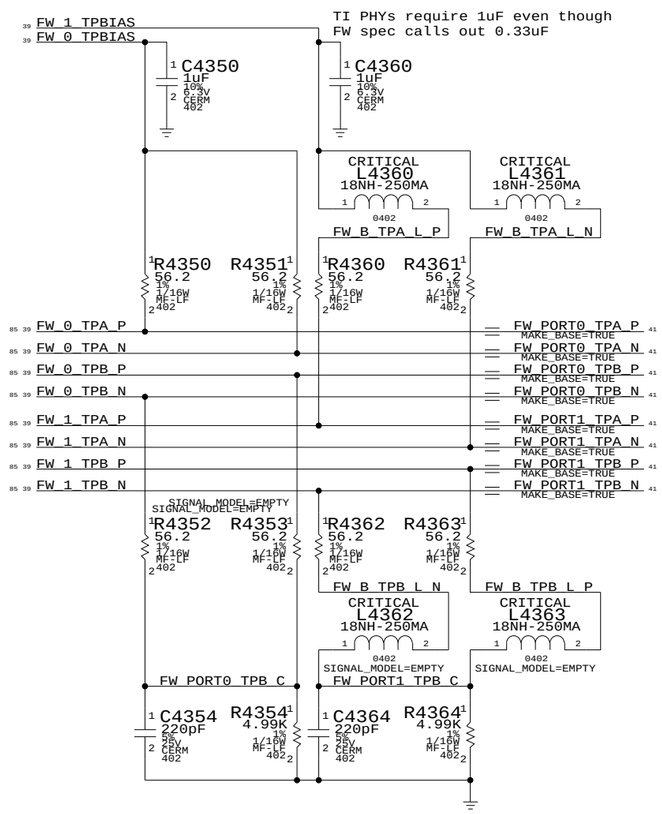
FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

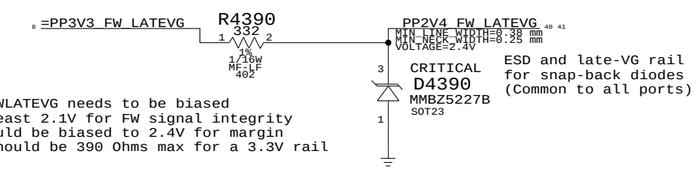


Termination

Place close to FireWire PHY



Late-VG Protection Power



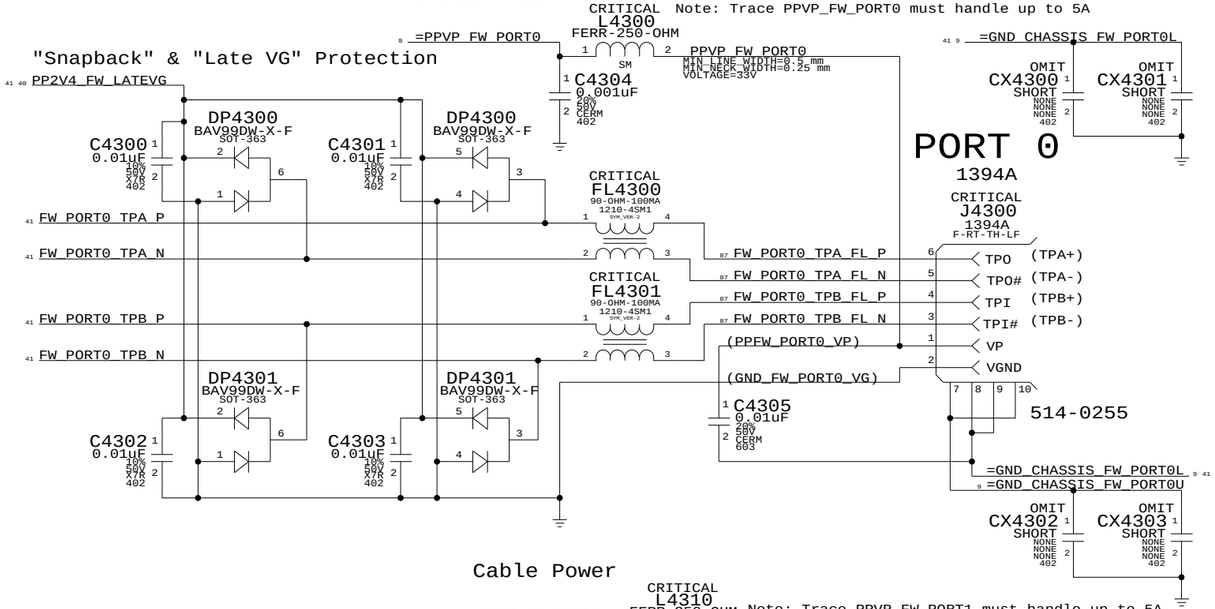
ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

Cable Power

Note: Trace PPVP_FW_PORT0 must handle up to 5A

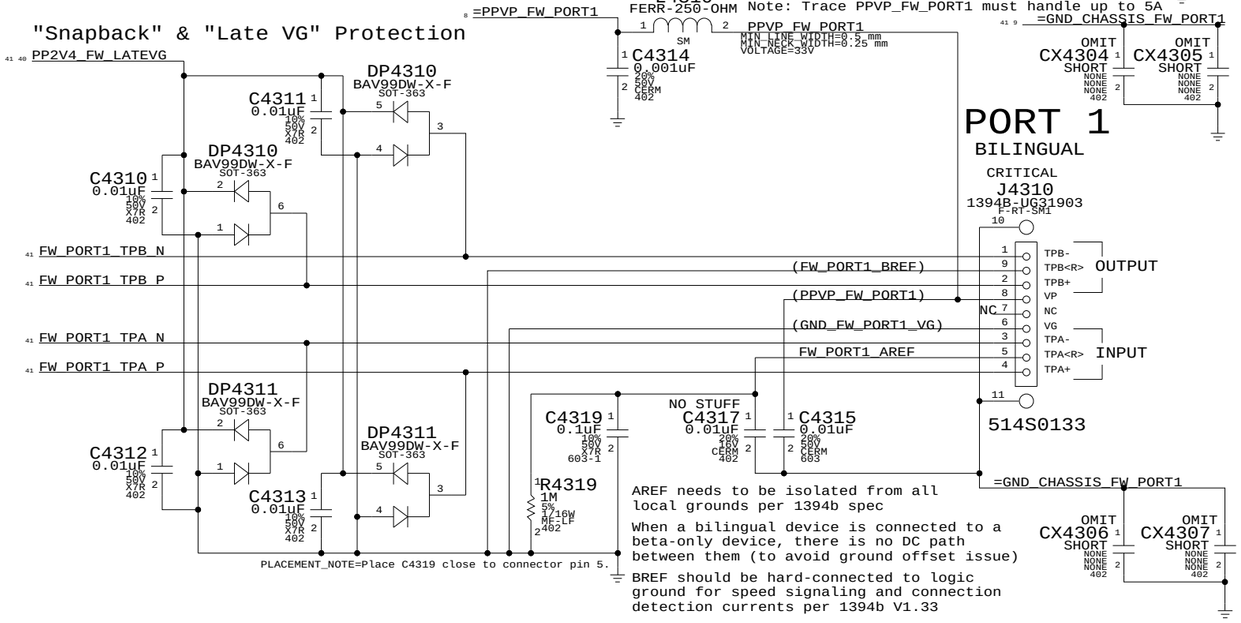
"Snapback" & "Late VG" Protection



Cable Power

Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

FireWire Ports

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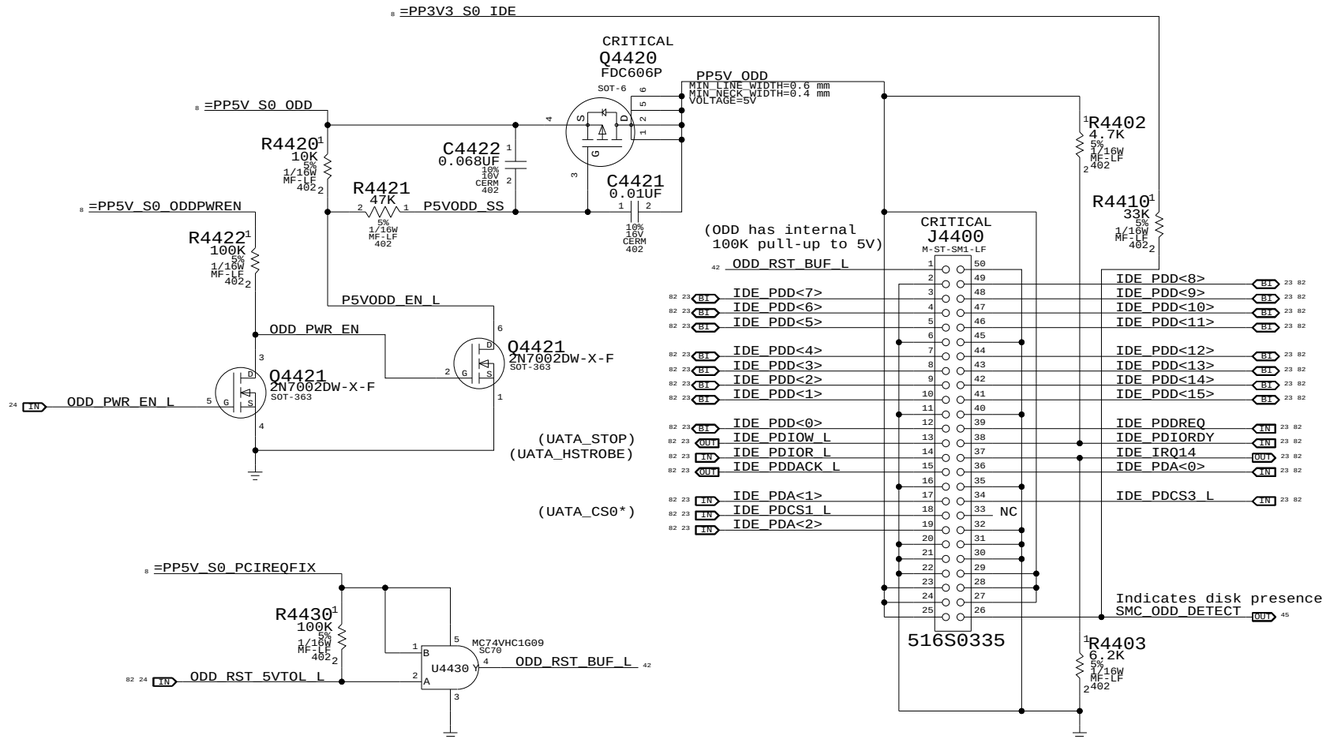
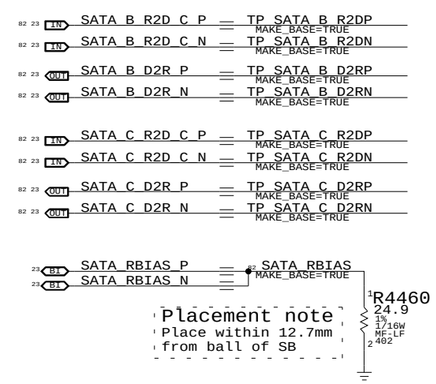
SCALE NONE	SHT 41 OF 88	

IDE (ODD) Connector



Unused SATA Ports



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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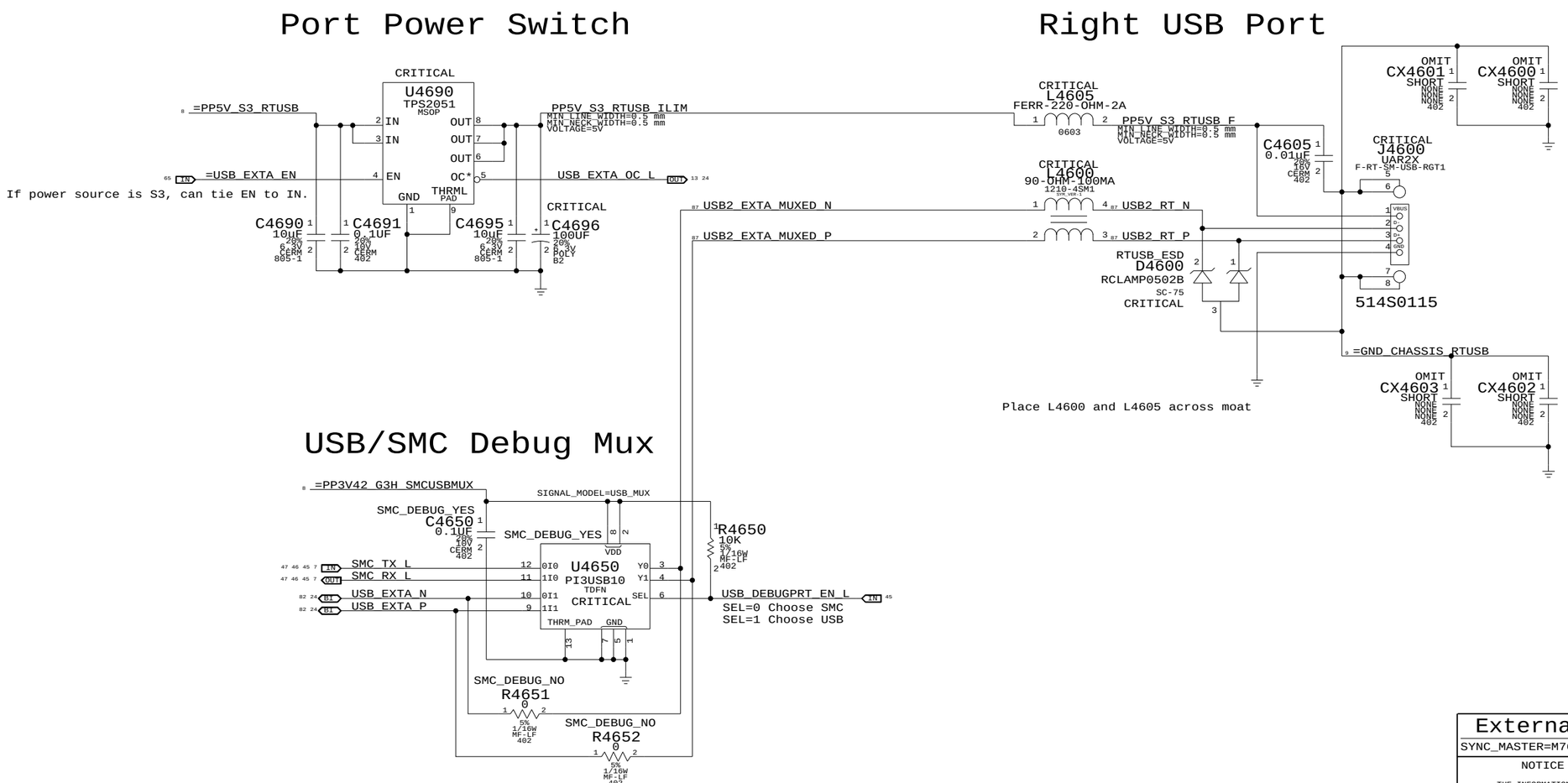
SCALE NONE — SHT 42 OF 88



External USB Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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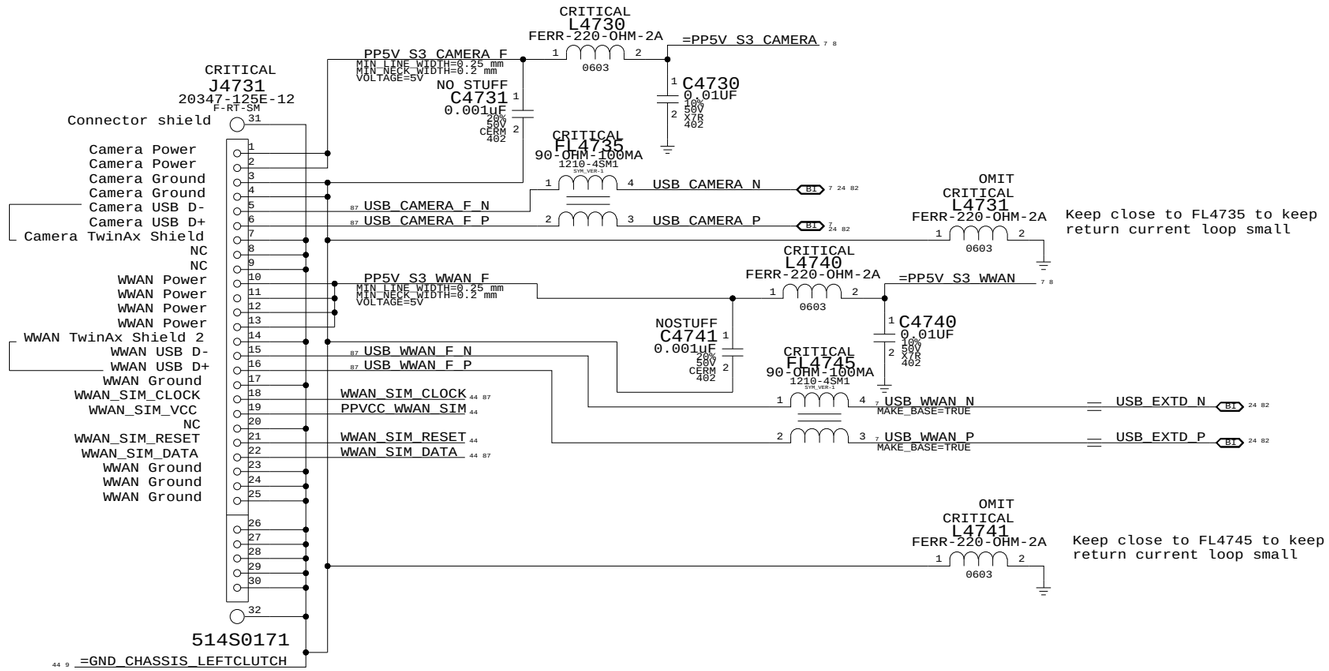
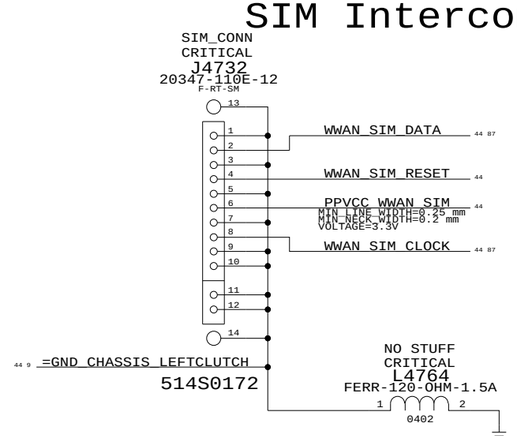
SCALE NONE	SHT 43 OF 88	

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SM,LF	L4731,L4741	CRITICAL	

SIM Interconnect



Left Clutch Barrel Interconnect

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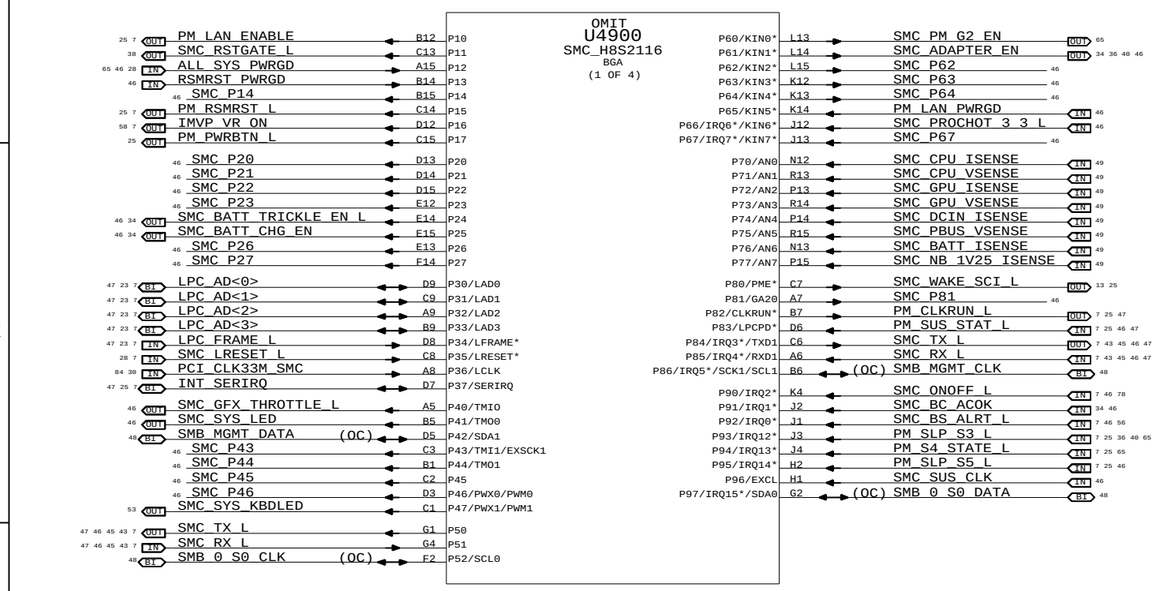
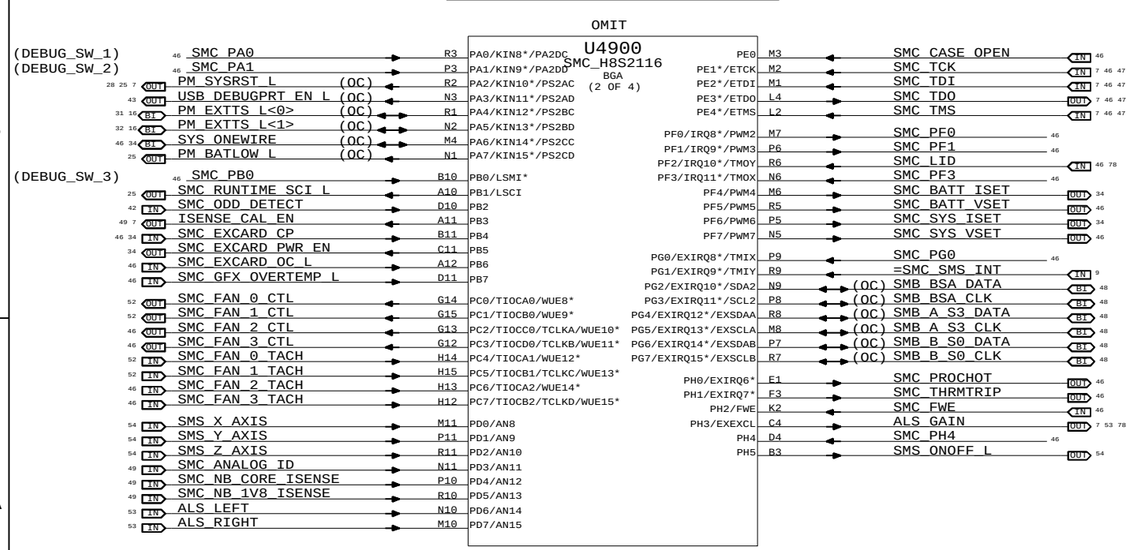
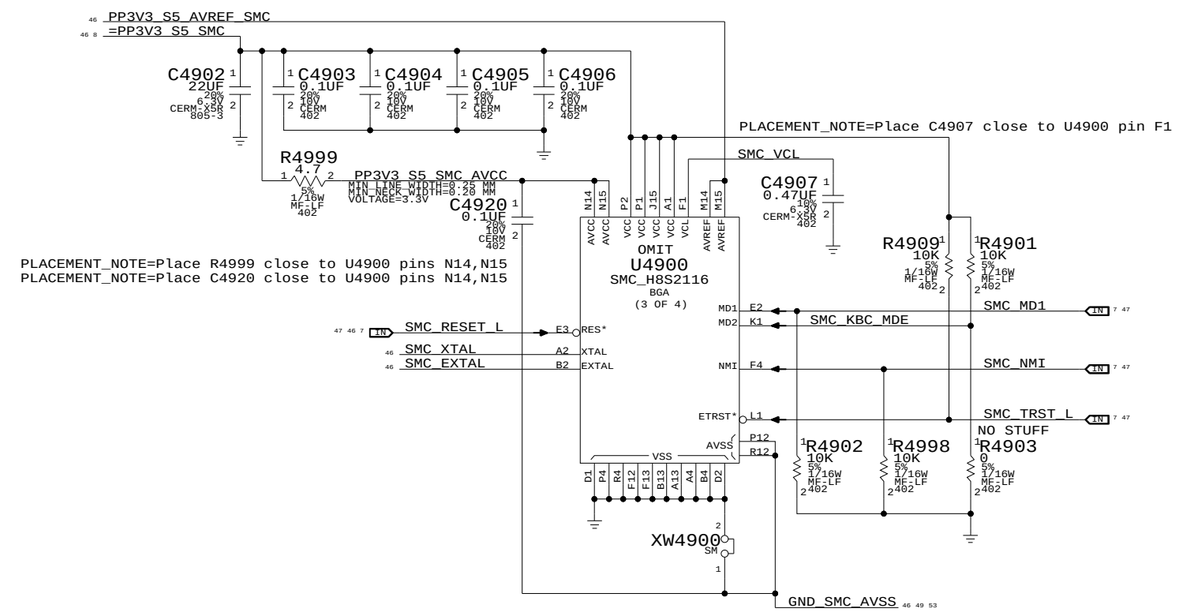
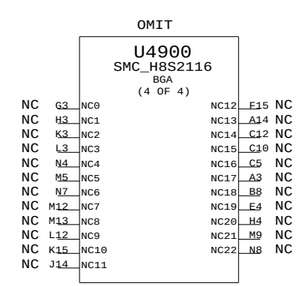
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007	

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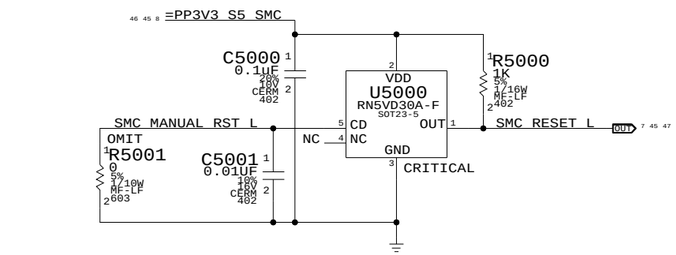
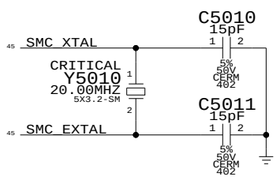
SCALE NONE	SHT 45 OF 88	

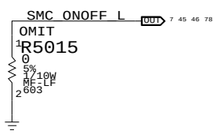
SMC Reset "Button" / Brownout Detect



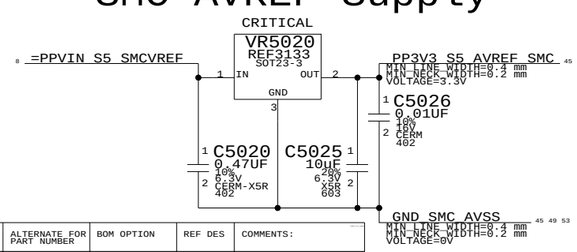
SMC Crystal Circuit



Debug Power "Button"

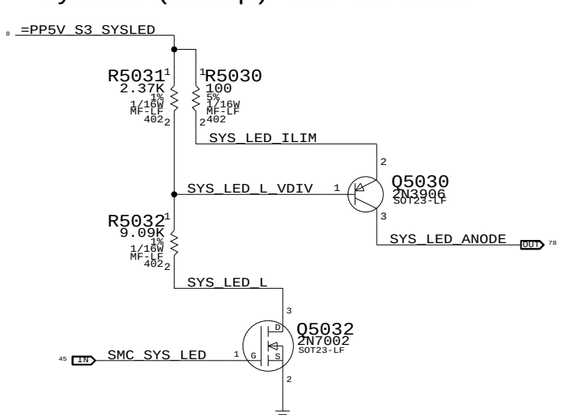


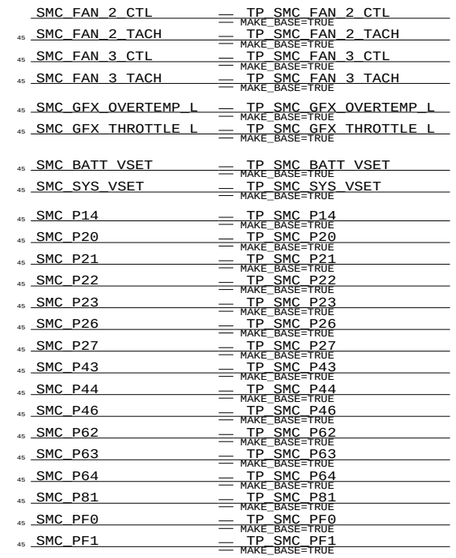
SMC AVREF Supply

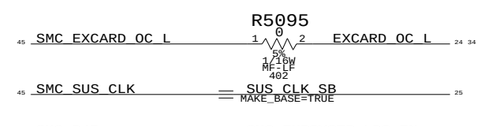


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

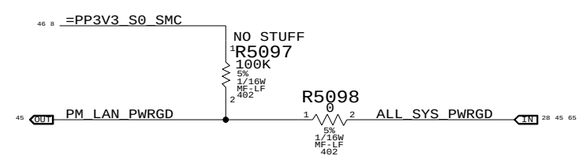
System (Sleep) LED Circuit





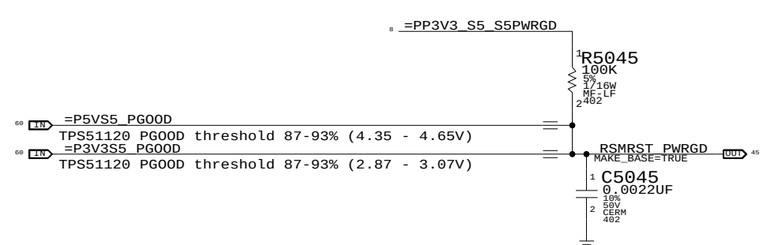


LAN PWRGD Circuit

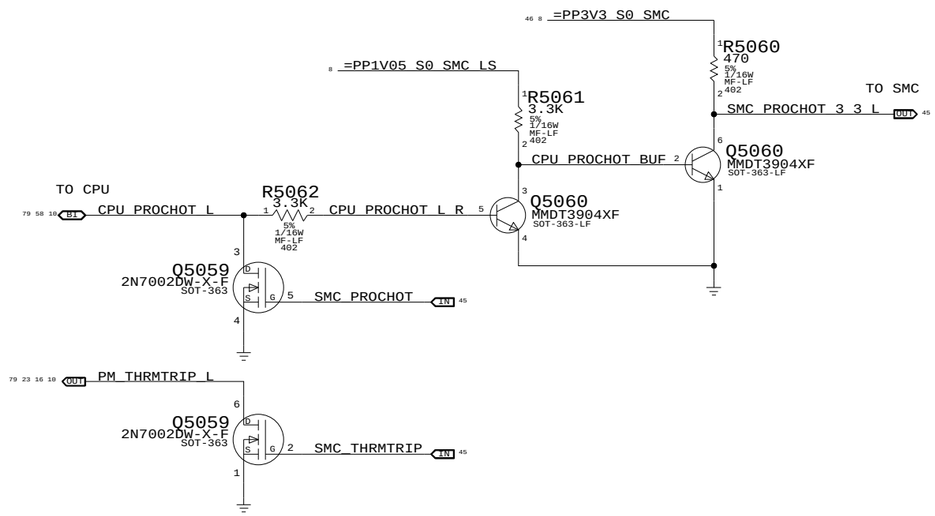


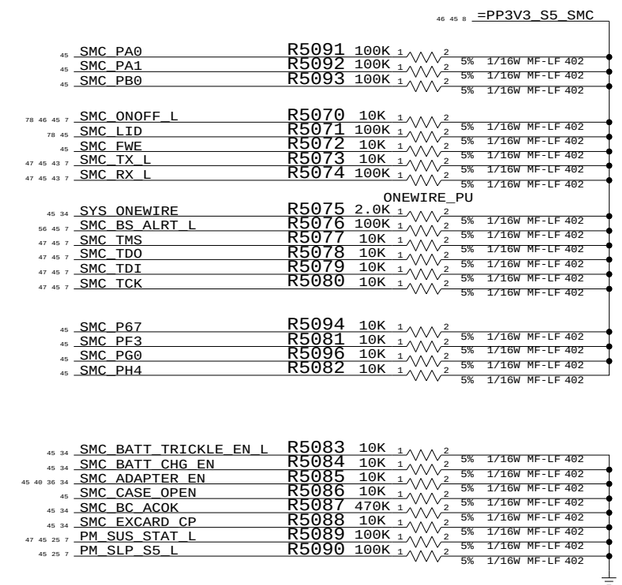
S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting





SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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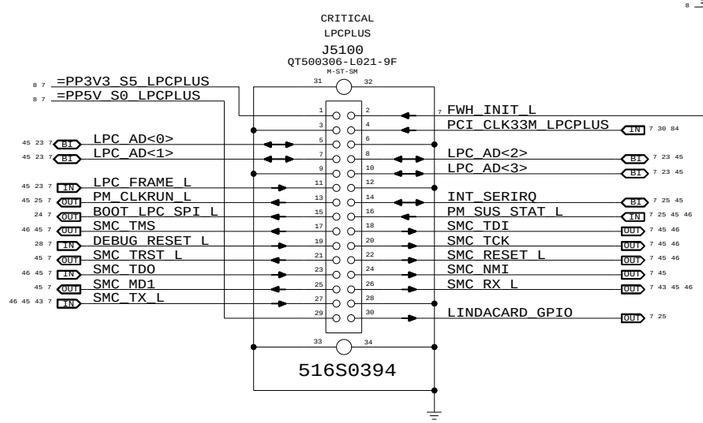
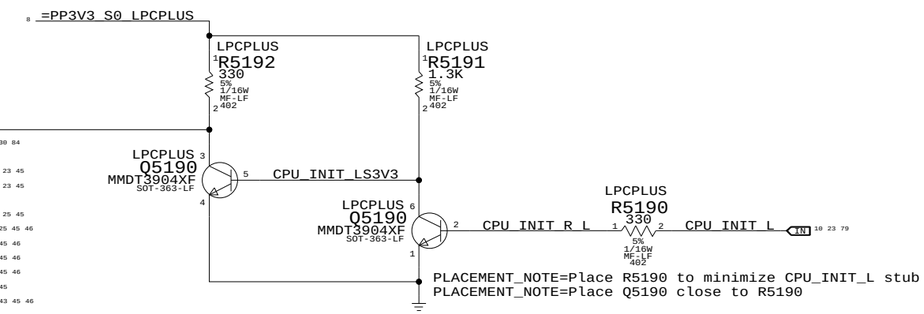
LPC+ Connector



FWH_INIT_L Generation



LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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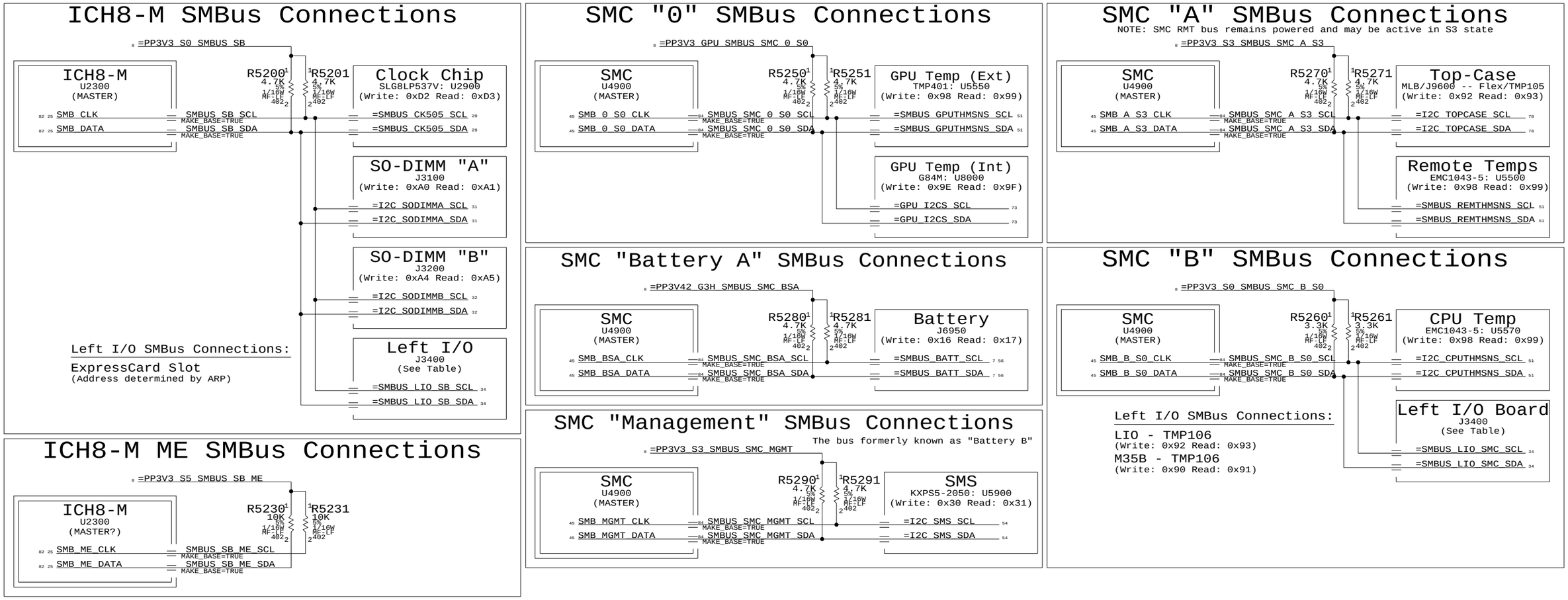

SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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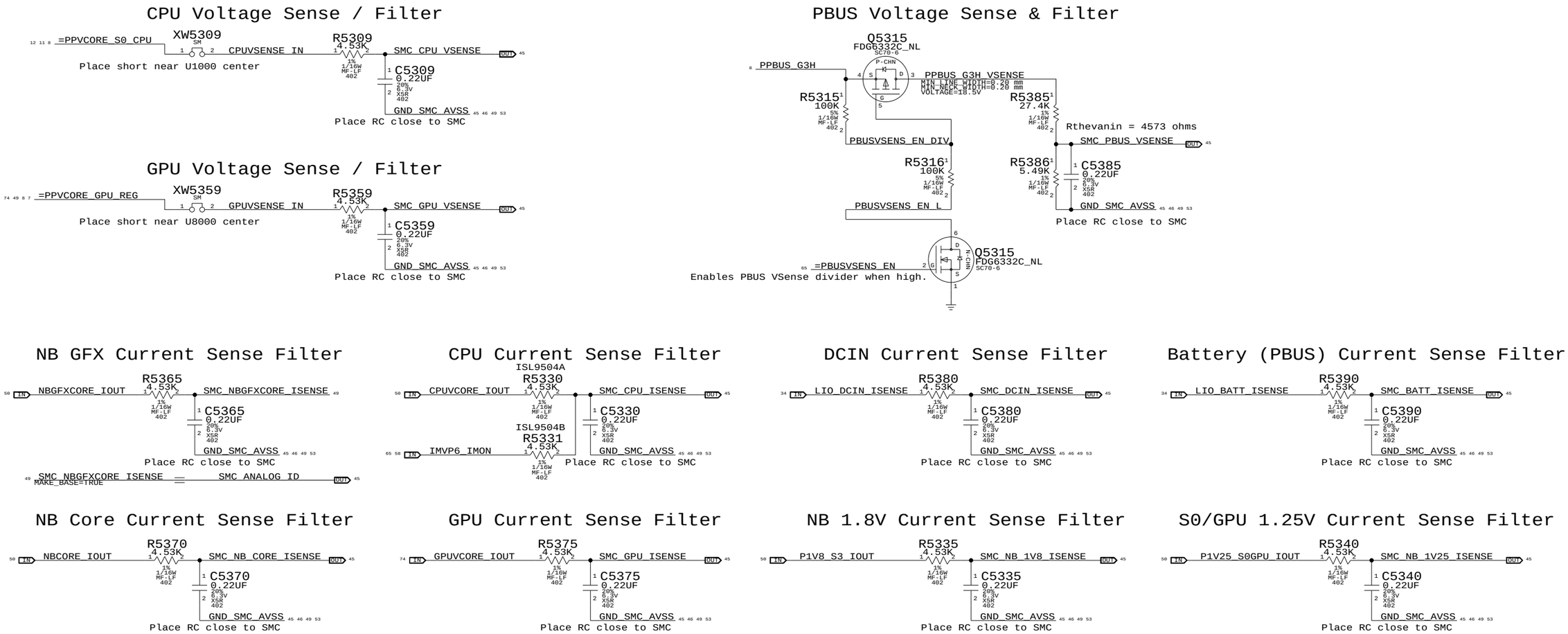
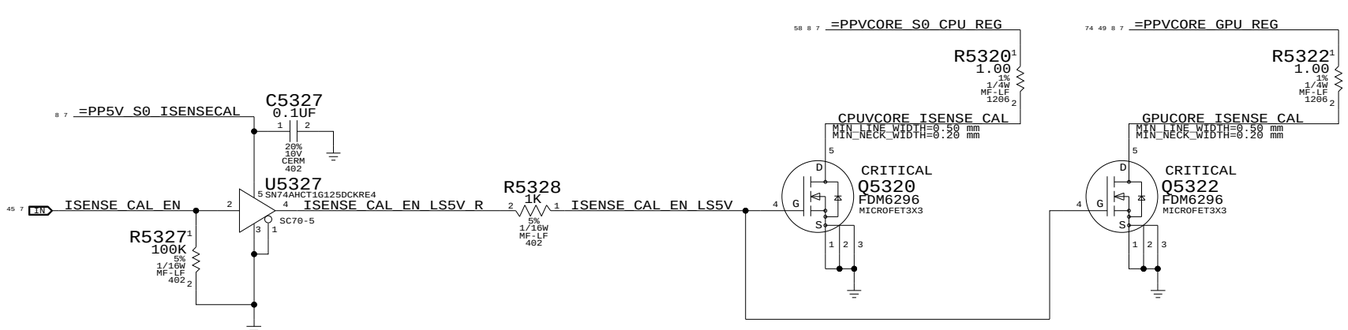


Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

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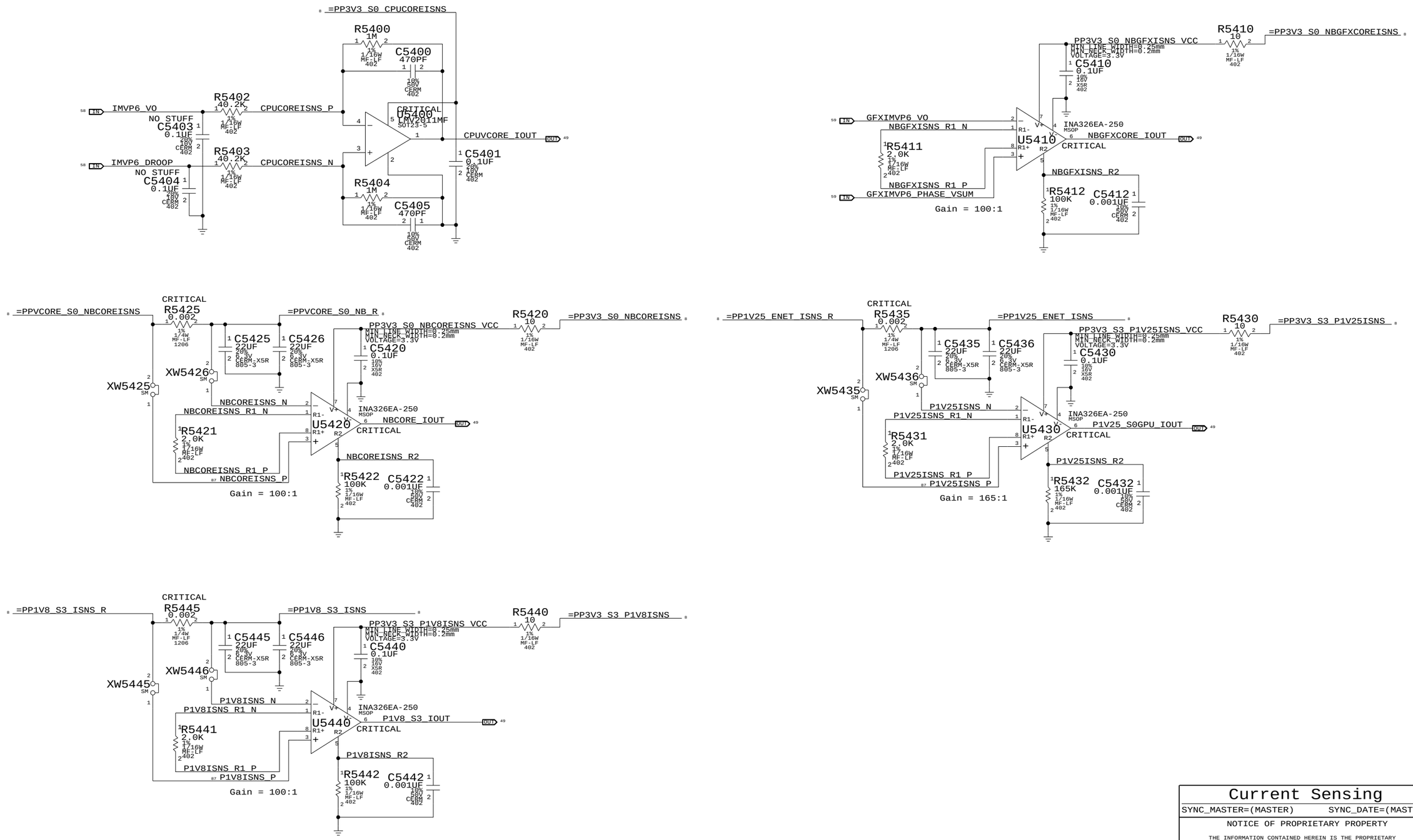
D	051-7225	A.0.0
SCALE NONE	SHT 49 OF 88	



Current Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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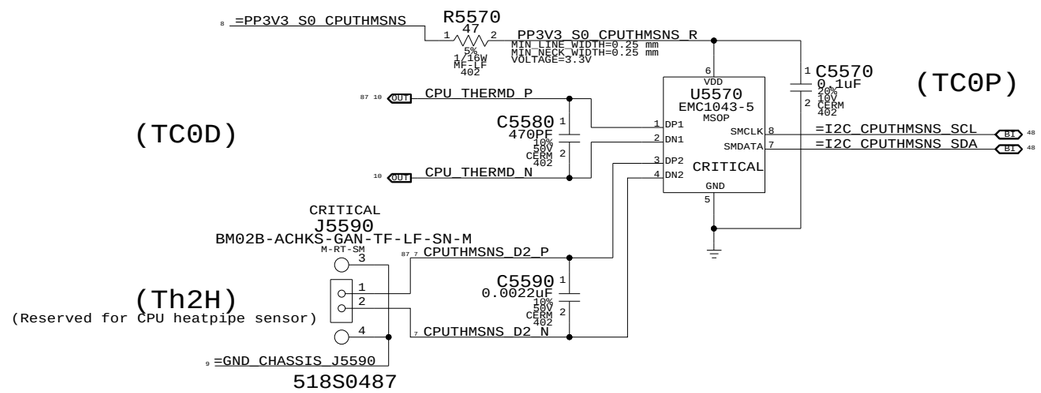
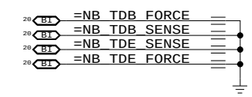
D	051-7225	A.0.0

SCALE NONE | SHT 50 OF 88

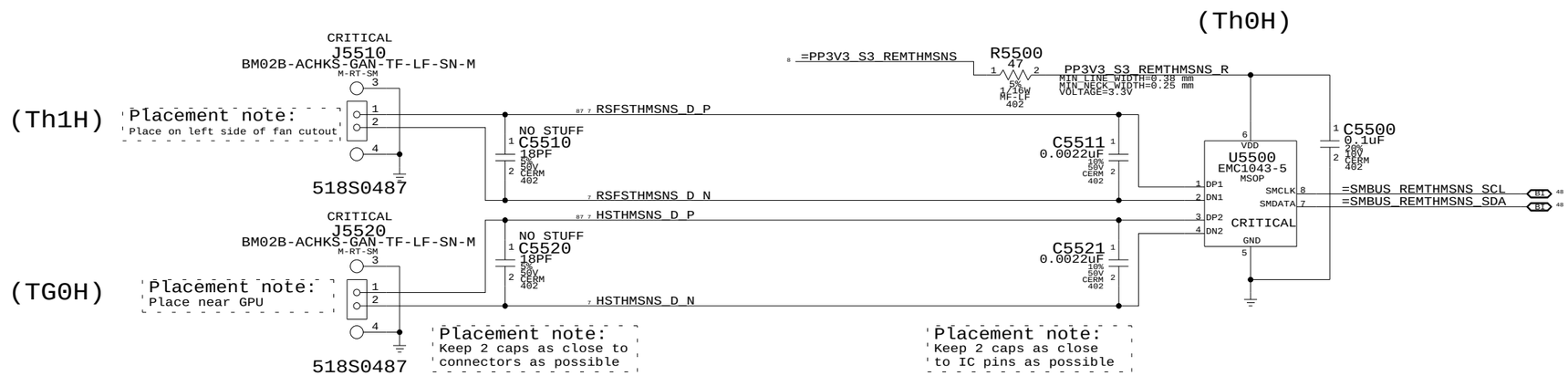
CPU T-Diode Thermal Sensor



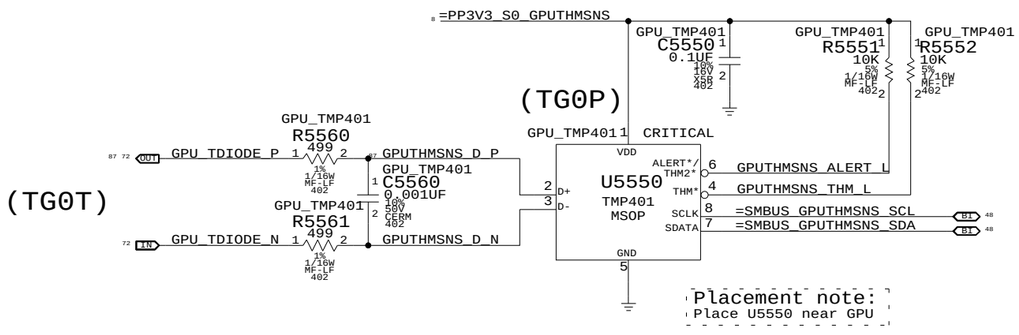
NB Thermal Diodes Not Used



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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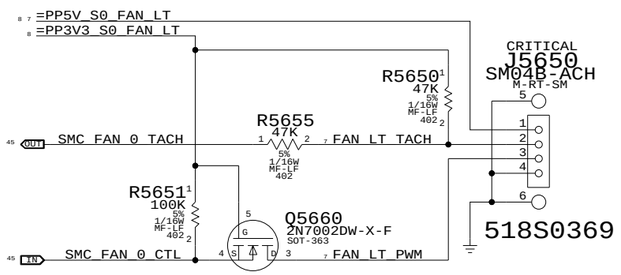
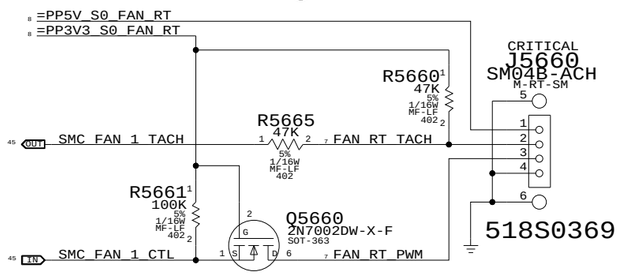
SCALE NONE

SHT 51 OF 88

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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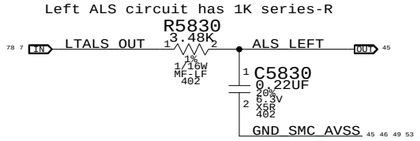
SCALE NONE

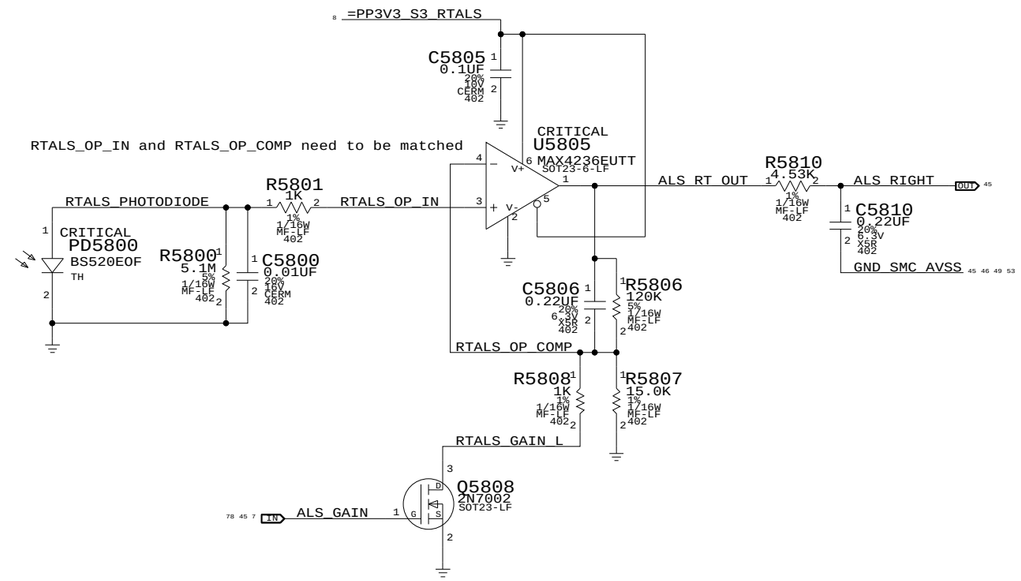
SHT 52 OF 88

Left ALS Filter

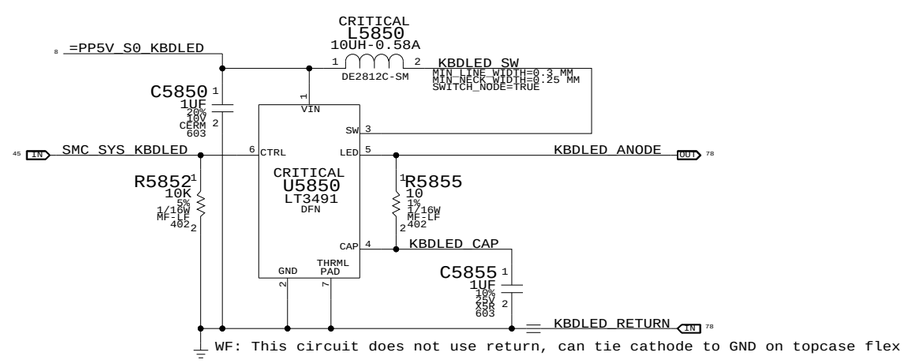
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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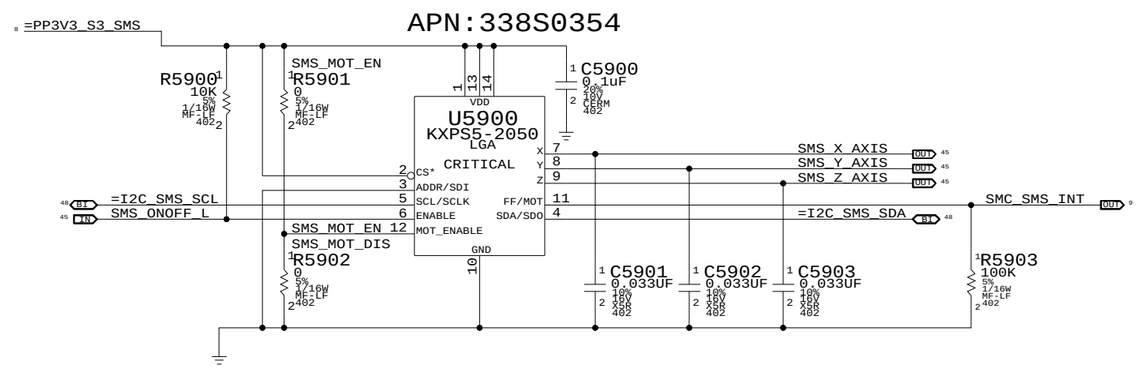
SCALE NONE	SHT 53 OF 88	



I2C addresses:

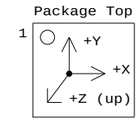
ADDR low => 0x30, 0x31

ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

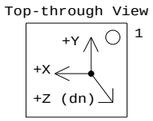
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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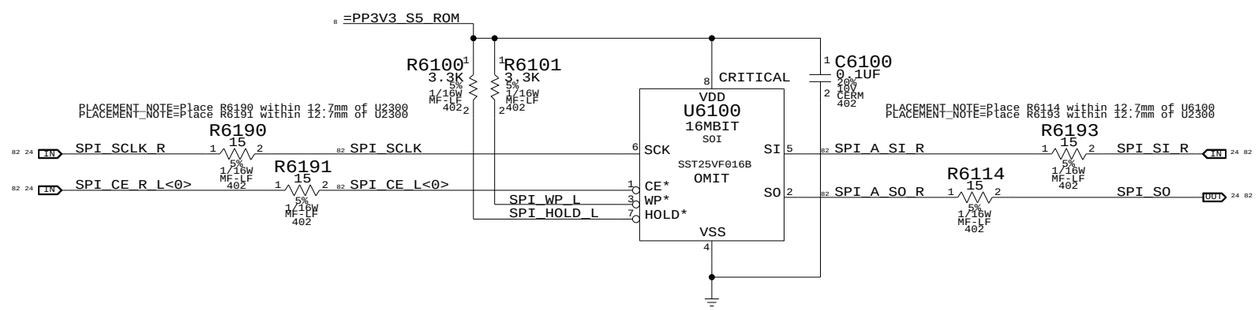
SCALE NONE

SHT 54 OF 88



SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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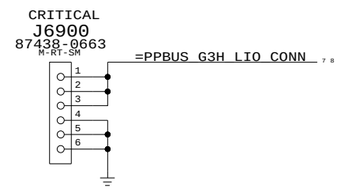
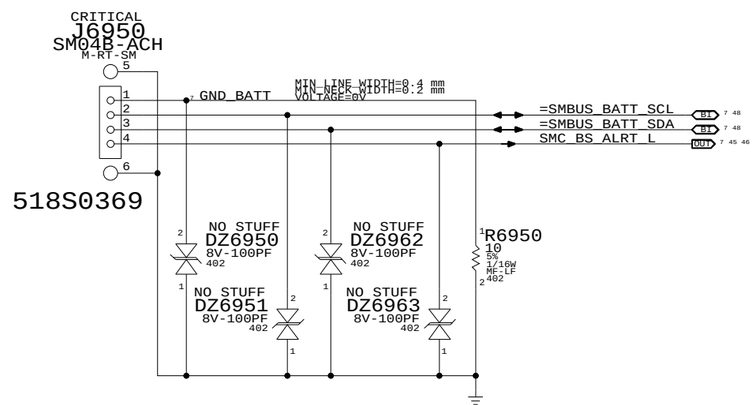
SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE NONE	SHT 55 OF 88	

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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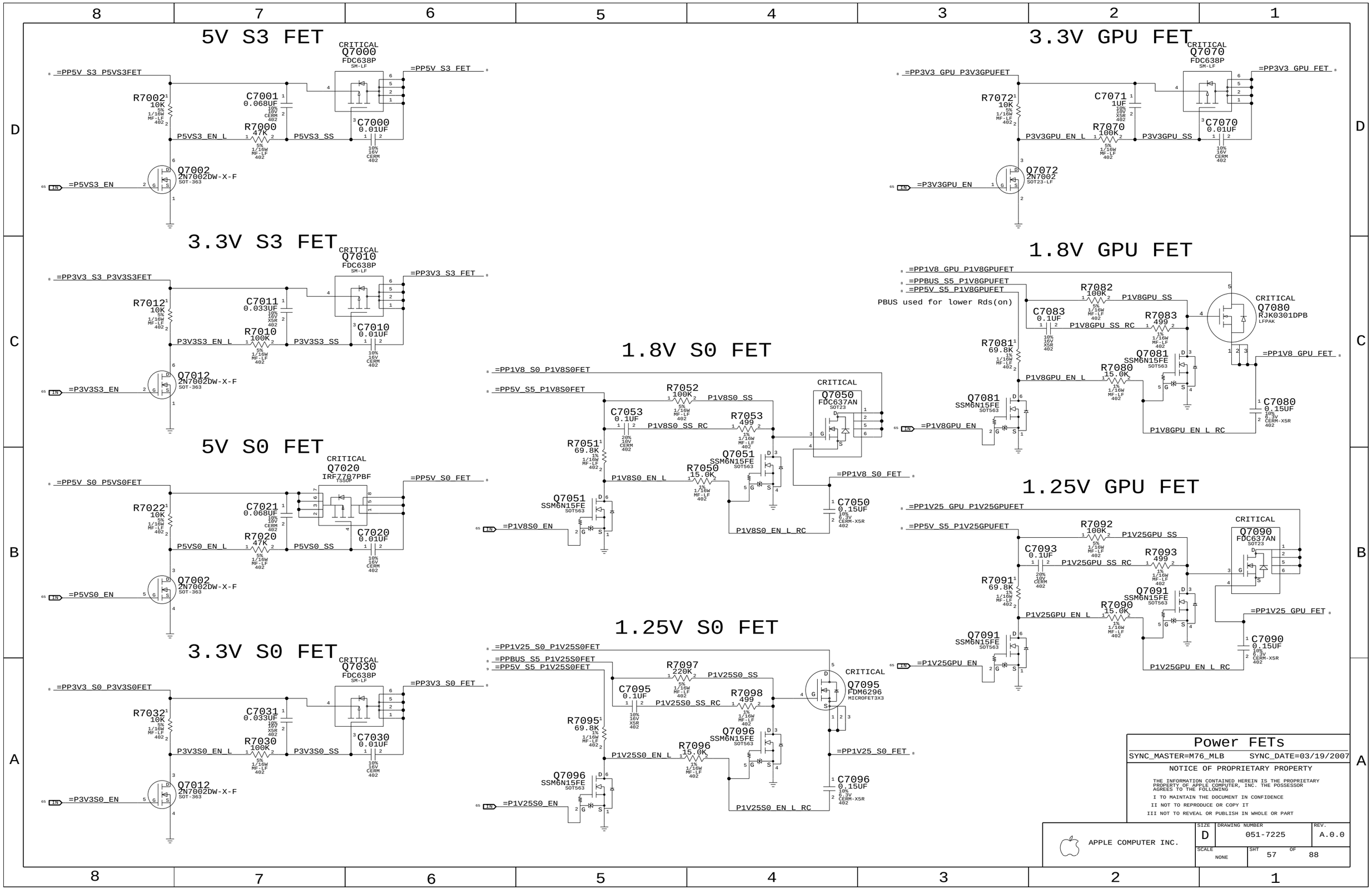
D	051-7225	A.0.0
SCALE NONE	SHT 56 OF 88	


5V S3 FET
=PP5V_S3_P5VS3FET
R7002 10K 5% 1/16W MF-LF 402
C7001 0.068UF 10% 16V CERM 402
R7000 47K 5% 1/16W MF-LF 402
P5VS3_EN_L
P5VS3_SS
CRITICAL
Q7000 FDC638P SM-LF
C7000 0.01UF 10% 16V CERM 402
=PP5V_S3_FET
Q7002 2N7002DW-X-F SOT-363
=P5VS3_EN
3.3V S3 FET
=PP3V3_S3_P3V3S3FET
R7012 10K 5% 1/16W MF-LF 402
C7011 0.033UF 10% 16V X5R 402
R7010 100K 5% 1/16W MF-LF 402
P3V3S3_EN_L
P3V3S3_SS
Q7010 FDC638P SM-LF
C7010 0.01UF 10% 16V CERM 402
=PP3V3_S3_FET
Q7012 2N7002DW-X-F SOT-363
=P3V3S3_EN
5V S0 FET
=PP5V_S0_P5VS0FET
R7022 10K 5% 1/16W MF-LF 402
C7021 0.068UF 10% 16V CERM 402
R7020 47K 5% 1/16W MF-LF 402
P5VS0_EN_L
P5VS0_SS
Q7020 IRF7707PBF TSSOP
C7020 0.01UF 10% 16V CERM 402
=PP5V_S0_FET
Q7002 2N7002DW-X-F SOT-363
=P5VS0_EN
3.3V S0 FET
=PP3V3_S0_P3V3S0FET
R7032 10K 5% 1/16W MF-LF 402
C7031 0.033UF 10% 16V X5R 402
R7030 100K 5% 1/16W MF-LF 402
P3V3S0_EN_L
P3V3S0_SS
Q7030 FDC638P SM-LF
C7030 0.01UF 10% 16V CERM 402
=PP3V3_S0_FET
Q7012 2N7002DW-X-F SOT-363
=P3V3S0_EN
1.8V S0 FET
=PP1V8_S0_P1V8S0FET
=PP5V_S5_P1V8S0FET
R7052 100K 5% 1/16W MF-LF 402
P1V8S0_SS
C7053 0.1UF 20% 10V CERM 402
P1V8S0_SS_RC
R7053 499 1% 1/16W MF-LF 402
R7051 69.8K 1% 1/16W MF-LF 402
Q7051 SSM6N15FE SOT563
R7050 15.0K 1% 1/16W MF-LF 402
P1V8S0_EN_L
Q7051 SSM6N15FE SOT563
CRITICAL
Q7050 FDC637AN SOT23
=PP1V8_S0_FET
C7050 0.15UF 10% 6.3V CERM-X5R 402
P1V8S0_EN_L_RC
=P1V8S0_EN
1.25V S0 FET
=PP1V25_S0_P1V25S0FET
=PPBUS_S5_P1V25S0FET
=PP5V_S5_P1V25S0FET
R7097 220K 5% 1/16W MF-LF 402
P1V25S0_SS
C7095 0.1UF 10% 16V X5R 402
P1V25S0_SS_RC
R7098 499 1% 1/16W MF-LF 402
R7095 69.8K 1% 1/16W MF-LF 402
Q7096 SSM6N15FE SOT563
R7096 15.0K 1% 1/16W MF-LF 402
P1V25S0_EN_L
Q7096 SSM6N15FE SOT563
CRITICAL
Q7095 FDM6296 MICROFET3X3
=PP1V25_S0_FET
C7096 0.15UF 10% 6.3V CERM-X5R 402
P1V25S0_EN_L_RC
=P1V25S0_EN
3.3V GPU FET
=PP3V3_GPU_P3V3GPUFET
R7072 10K 5% 1/16W MF-LF 402
C7071 1UF 10% 16V X5R 402
R7070 100K 5% 1/16W MF-LF 402
P3V3GPU_EN_L
P3V3GPU_SS
Q7070 FDC638P SM-LF
C7070 0.01UF 10% 16V CERM 402
=PP3V3_GPU_FET
Q7072 2N7002 SOT23-LF
=P3V3GPU_EN
1.8V GPU FET
=PP1V8_GPU_P1V8GPUFET
=PPBUS_S5_P1V8GPUFET
=PP5V_S5_P1V8GPUFET
PBUS used for lower Rds(on)
R7082 100K 5% 1/16W MF-LF 402
P1V8GPU_SS
C7083 0.1UF 10% 16V X5R 402
P1V8GPU_SS_RC
R7083 499 1% 1/16W MF-LF 402
CRITICAL
Q7080 RJK0301DPB LFPAK
R7081 69.8K 1% 1/16W MF-LF 402
Q7081 SSM6N15FE SOT563
R7080 15.0K 1% 1/16W MF-LF 402
P1V8GPU_EN_L
Q7081 SSM6N15FE SOT563
=PP1V8_GPU_FET
C7080 0.15UF 10% 6.3V CERM-X5R 402
P1V8GPU_EN_L_RC
=P1V8GPU_EN
1.25V GPU FET
=PP1V25_GPU_P1V25GPUFET
=PP5V_S5_P1V25GPUFET
R7092 100K 5% 1/16W MF-LF 402
P1V25GPU_SS
C7093 0.1UF 20% 10V CERM 402
P1V25GPU_SS_RC
R7093 499 1% 1/16W MF-LF 402
CRITICAL
Q7090 FDC637AN SOT23
R7091 69.8K 1% 1/16W MF-LF 402
Q7091 SSM6N15FE SOT563
R7090 15.0K 1% 1/16W MF-LF 402
P1V25GPU_EN_L
Q7091 SSM6N15FE SOT563
=PP1V25_GPU_FET
C7090 0.15UF 10% 6.3V CERM-X5R 402
P1V25GPU_EN_L_RC
=P1V25GPU_EN
Power FETs
SYNC_MASTER=M76_MLB
SYNC_DATE=03/19/2007
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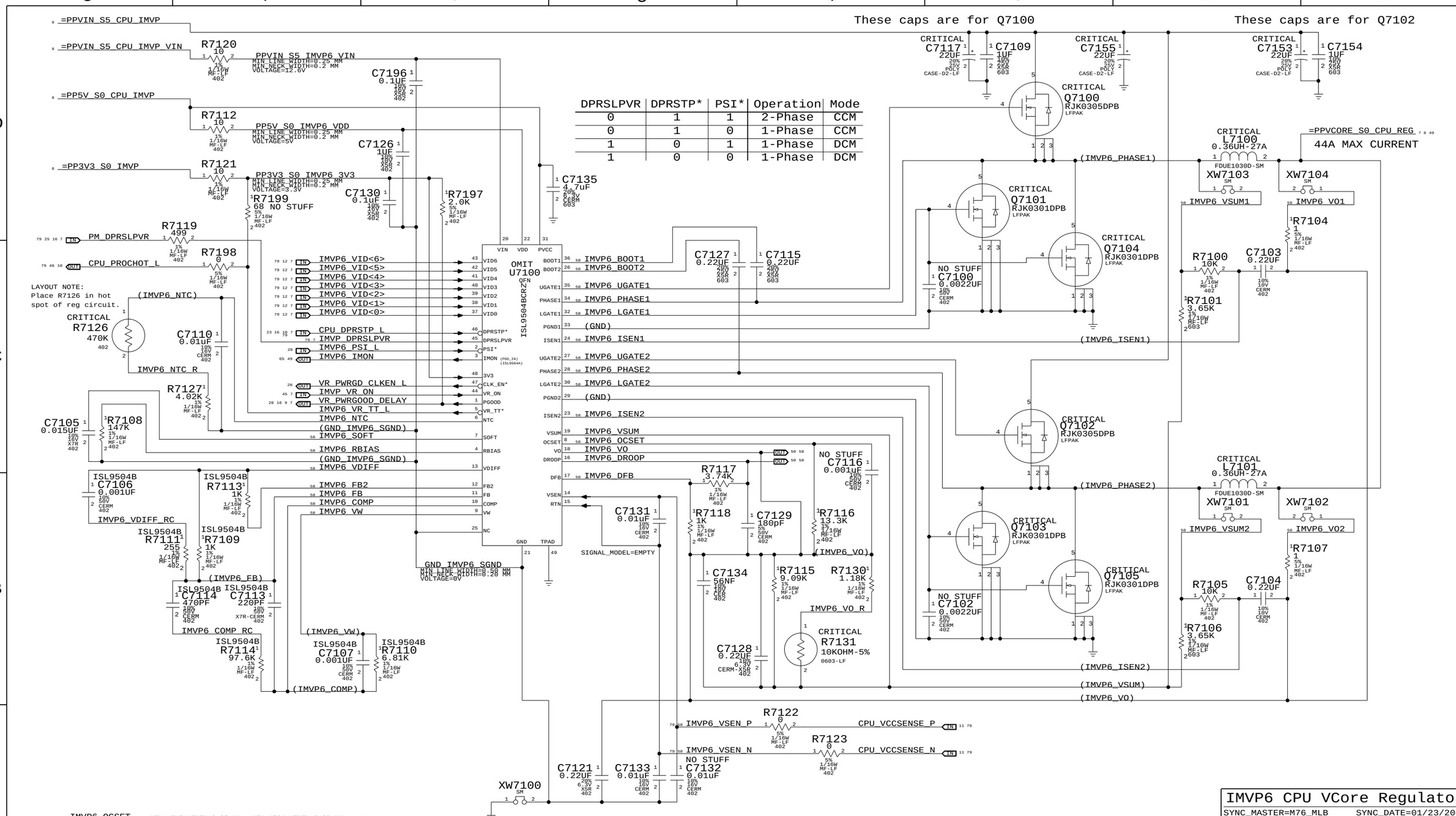
SIZE D
DRAWING NUMBER 051-7225
REV. A.0.0
SCALE NONE
SHT 57 OF 88



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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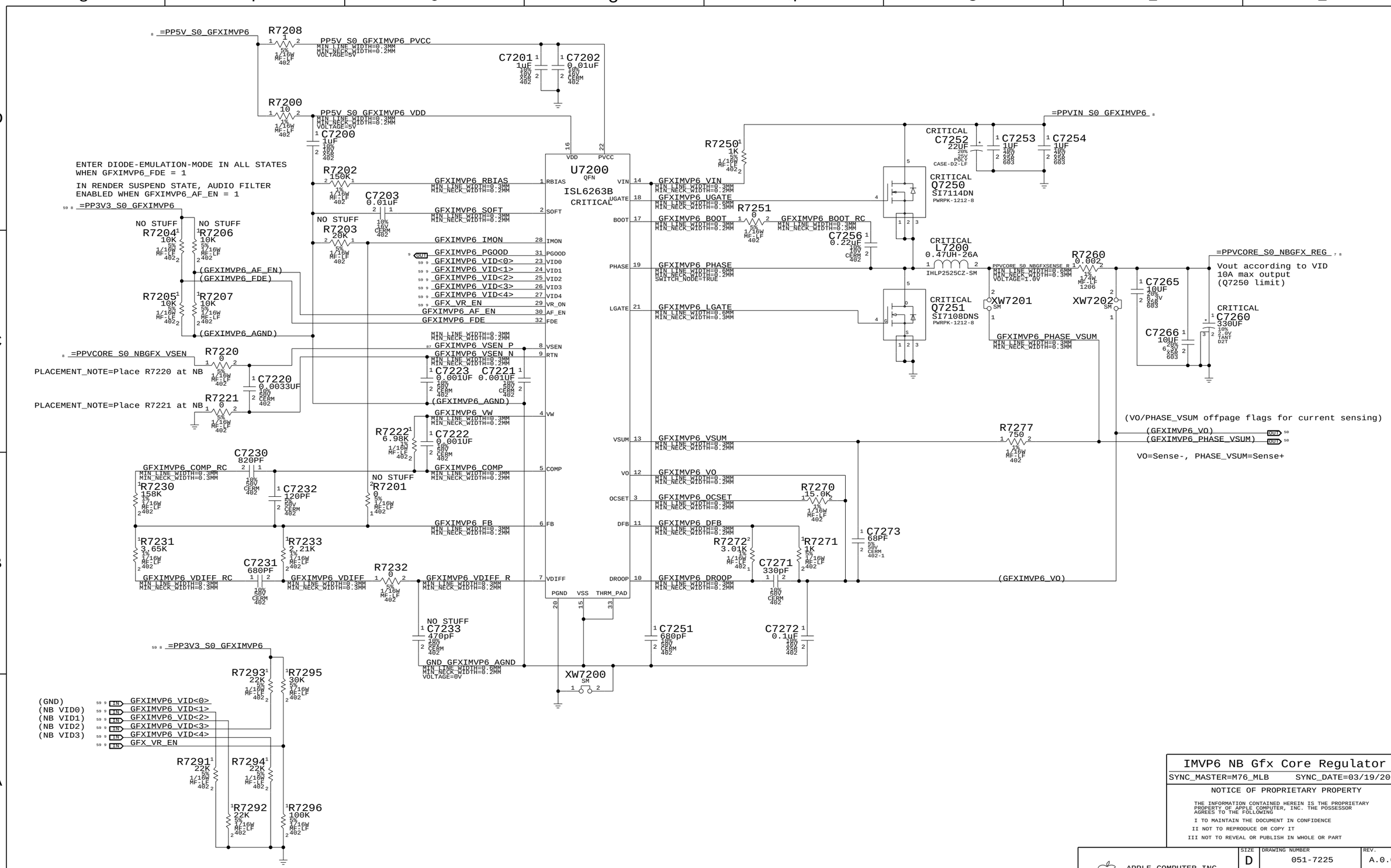
SCALE NONE	SHT 58 OF 88	



NOTE: Intel recommendation to stuff 30K pull-up and
100K pull-down on VR_EN per Crestline Issue #306022.

IMVP6 NB Gfx Core Regulator

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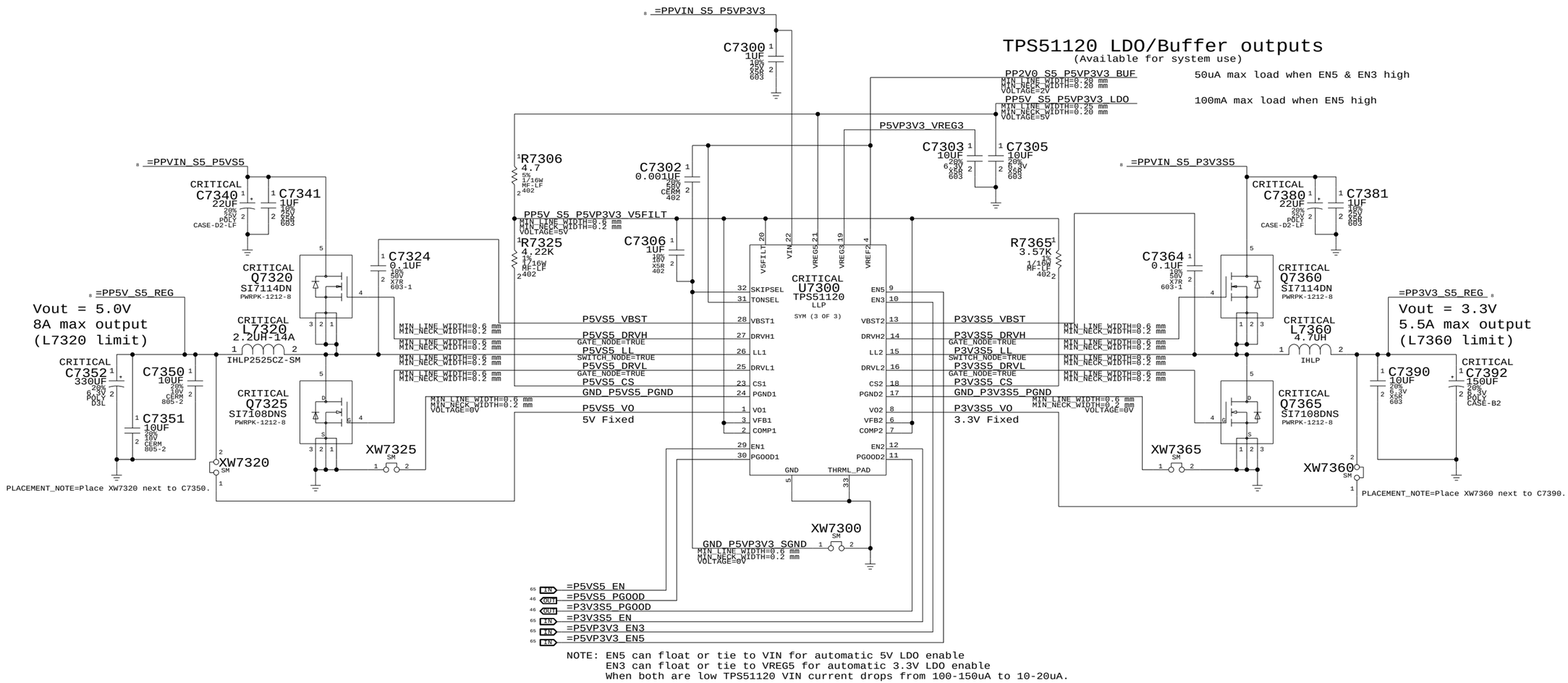
SCALE NONE

SHT 59 OF 88



NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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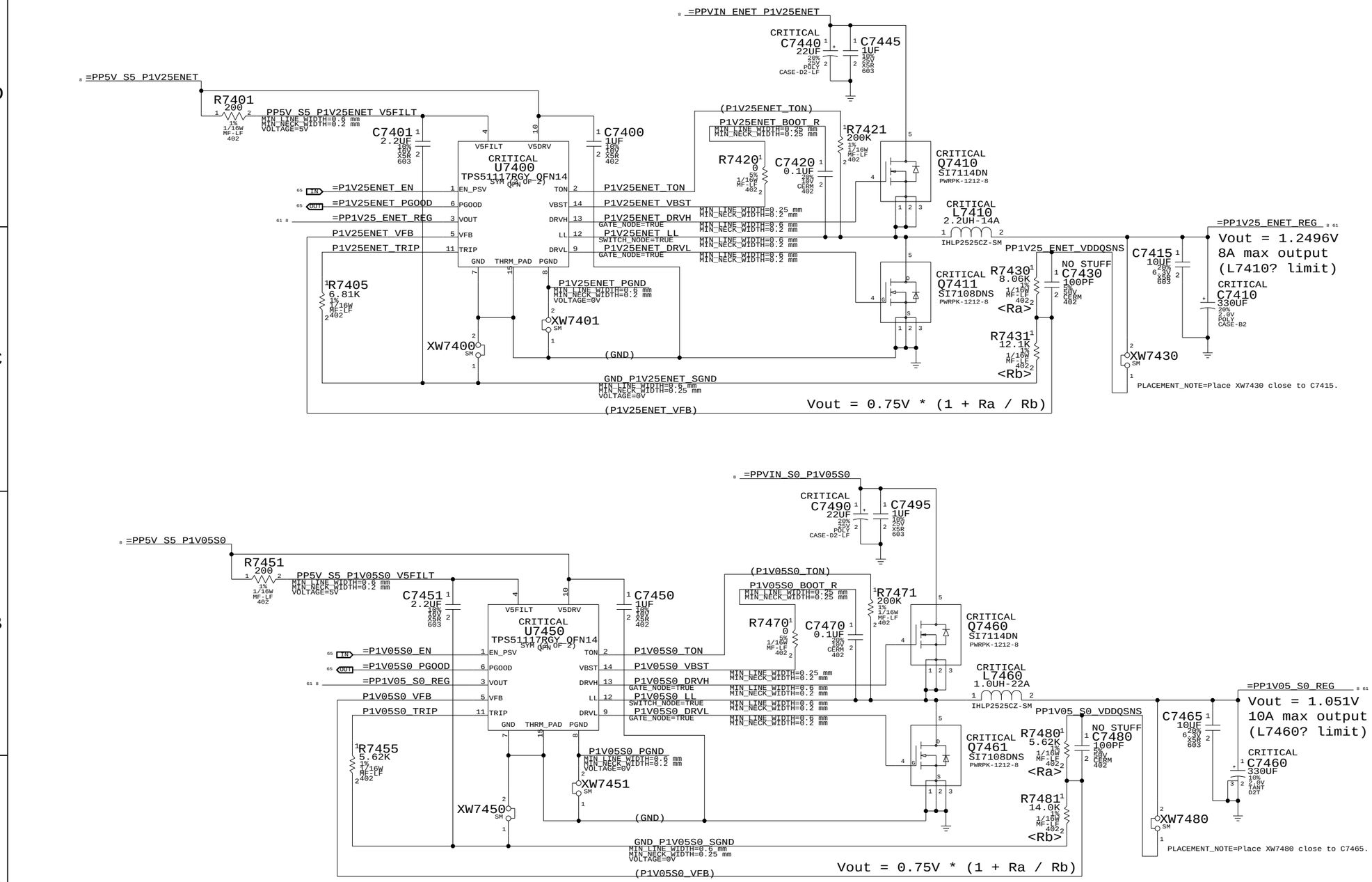
SCALE NONE SHT 60 OF 88



1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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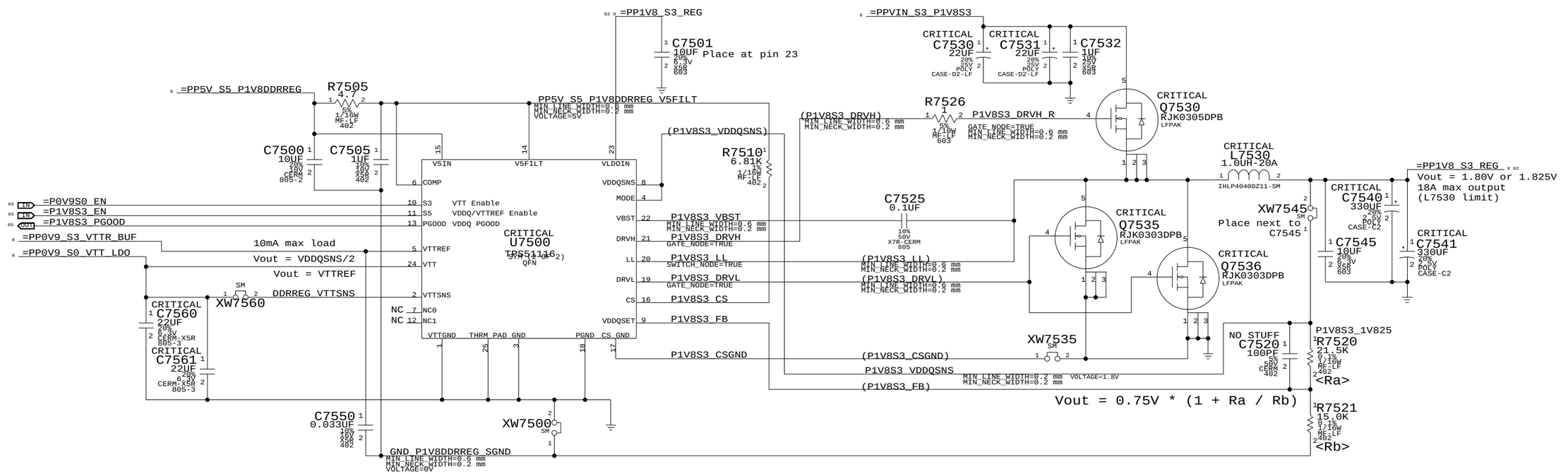
SCALE NONE	SHT 61 OF 88	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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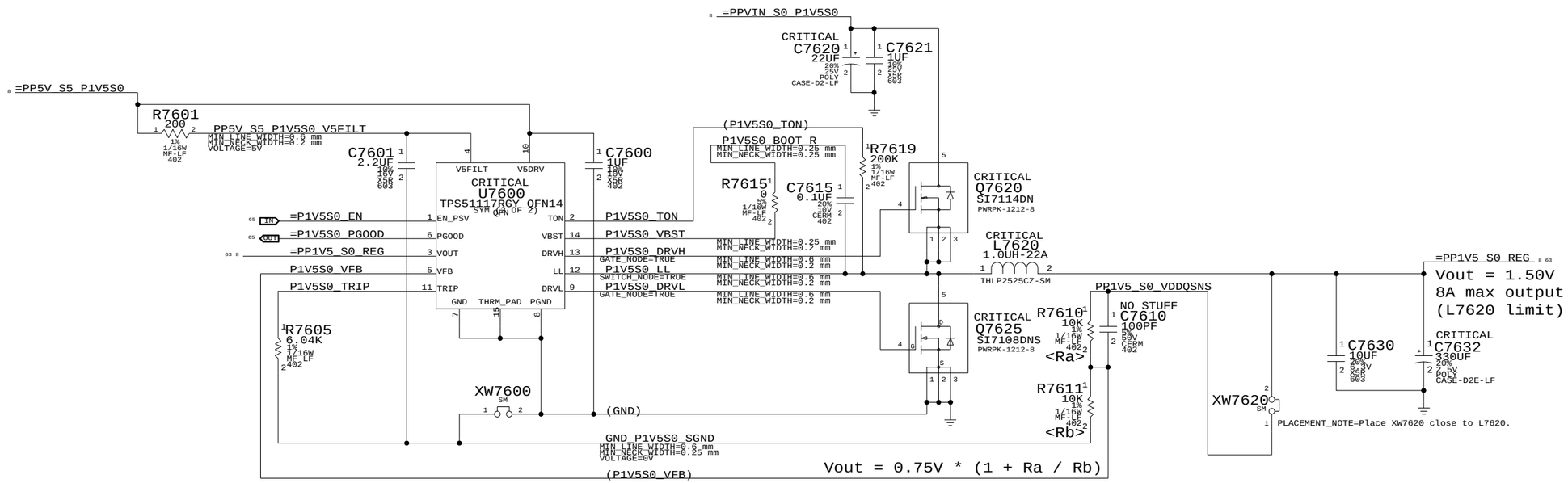
SCALE NONE SHT 62 OF 88



1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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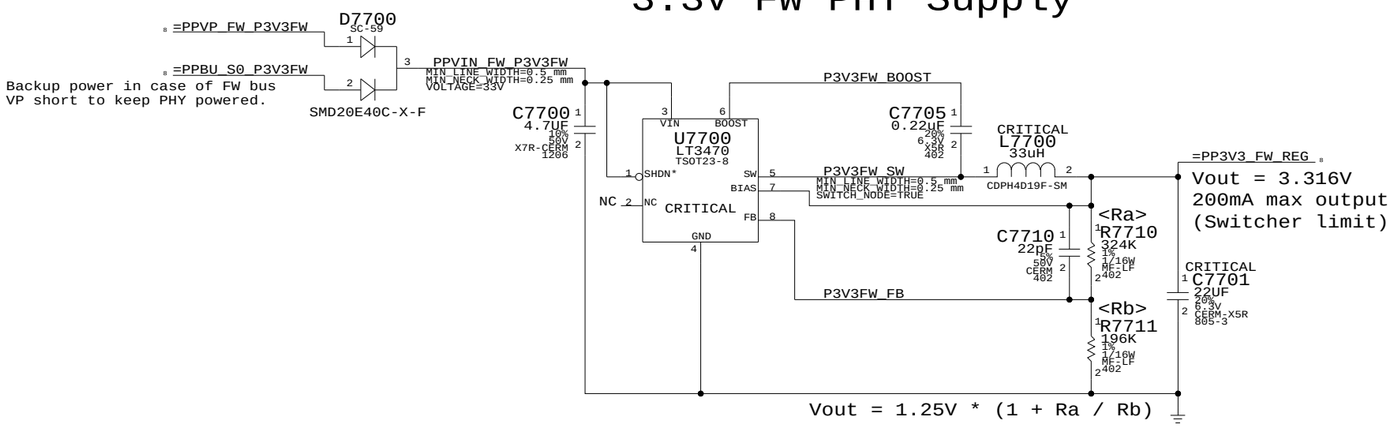
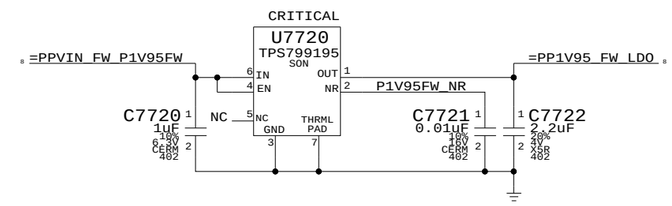
SCALE NONE

SHT 63 OF 88

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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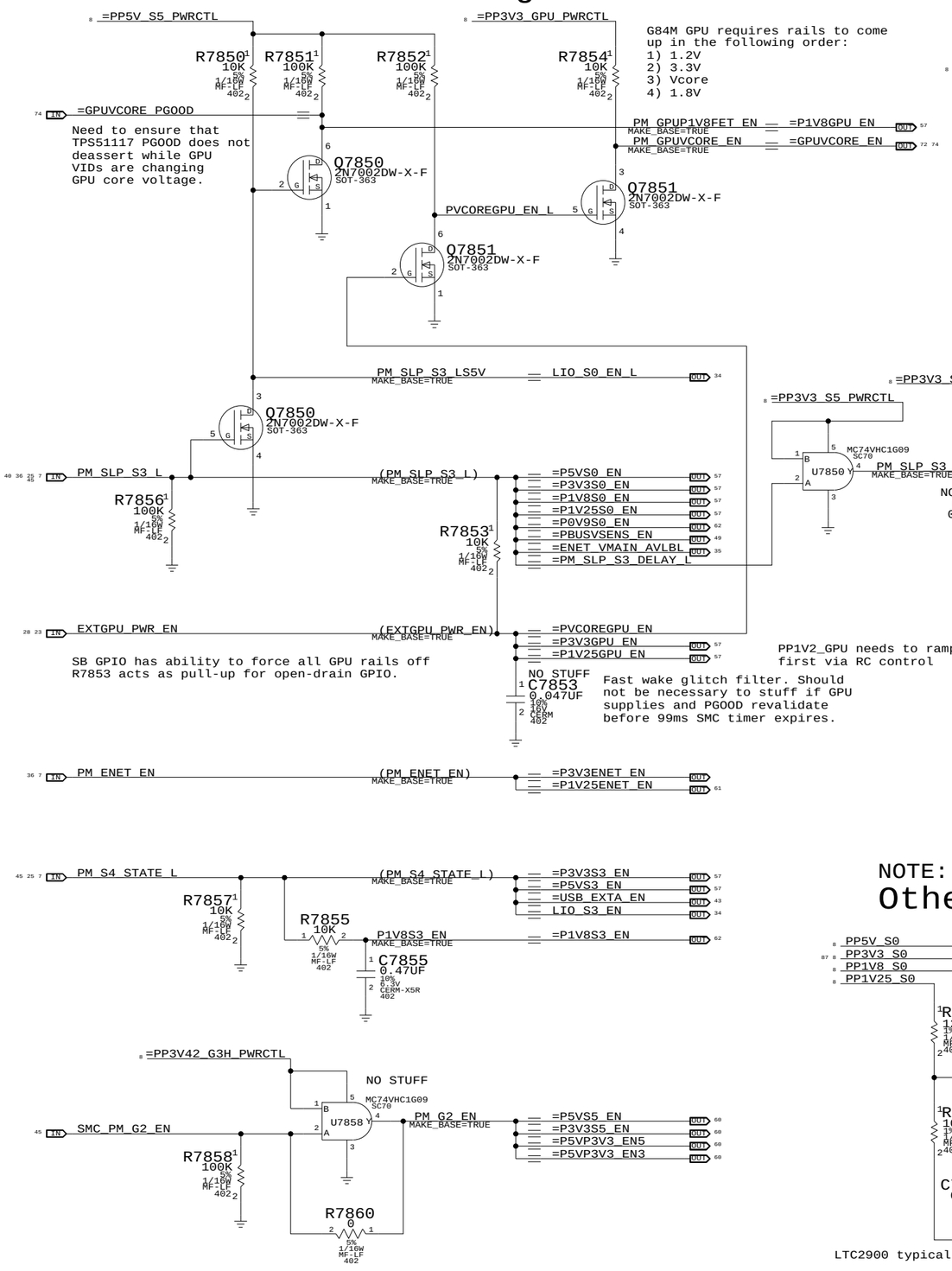
SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE NONE	SHT 64 OF 88	

Power Control Signals



G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

SB GPIO has ability to force all GPU rails off
R7853 acts as pull-up for open-drain GPIO.

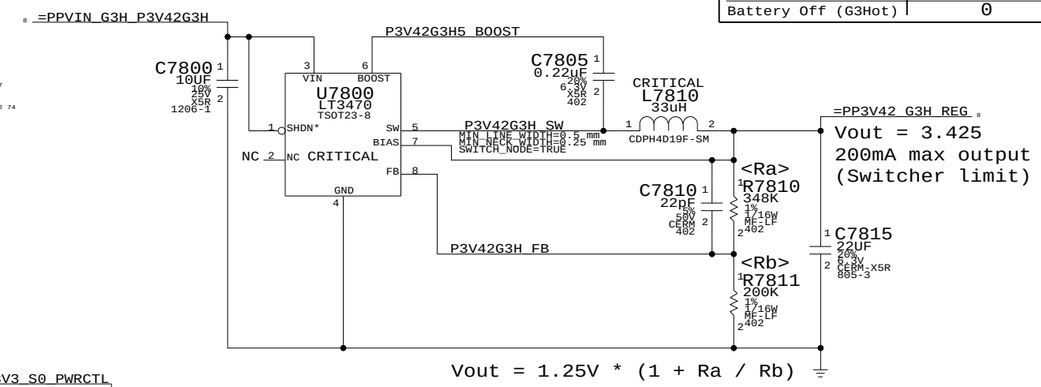
PP1V2_GPU needs to ramp first via RC control

Fast wake glitch filter. Should not be necessary to stuff if GPU supplies and PGOOD revalidate before 99ms SMC timer expires.

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

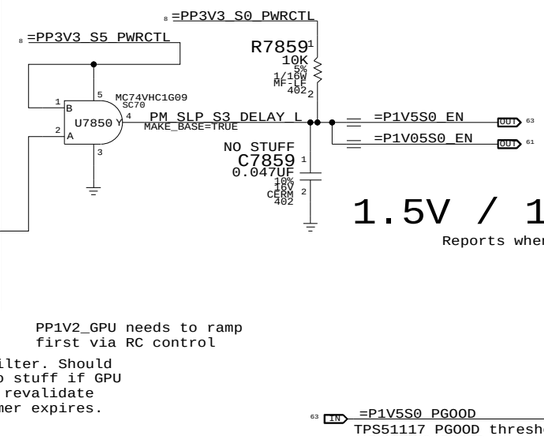
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



Vout = 1.25V * (1 + Ra / Rb)

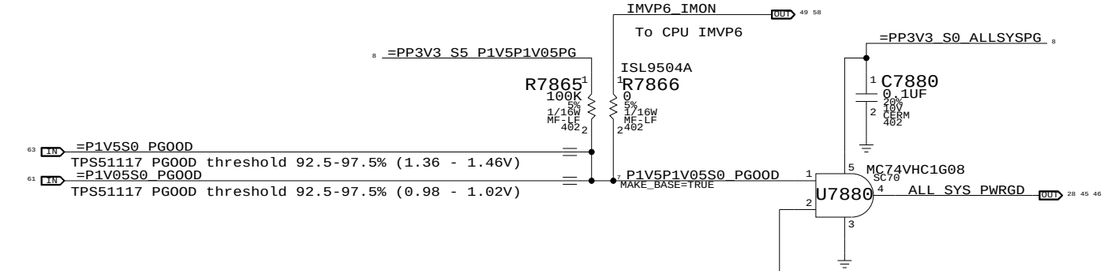
1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



Unused PGOOD Signals

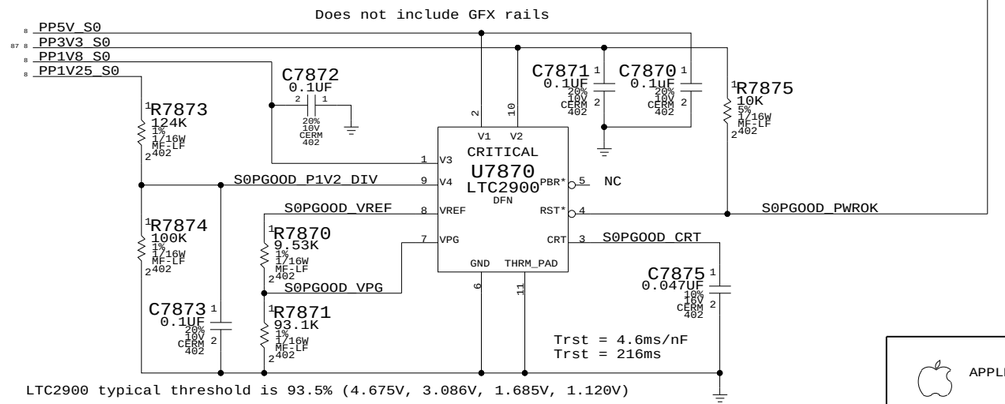
=P1V25ENET_PGOOD — TP_P1V25ENET_PGOOD (MAKE_BASE=TRUE)
=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)



NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails



LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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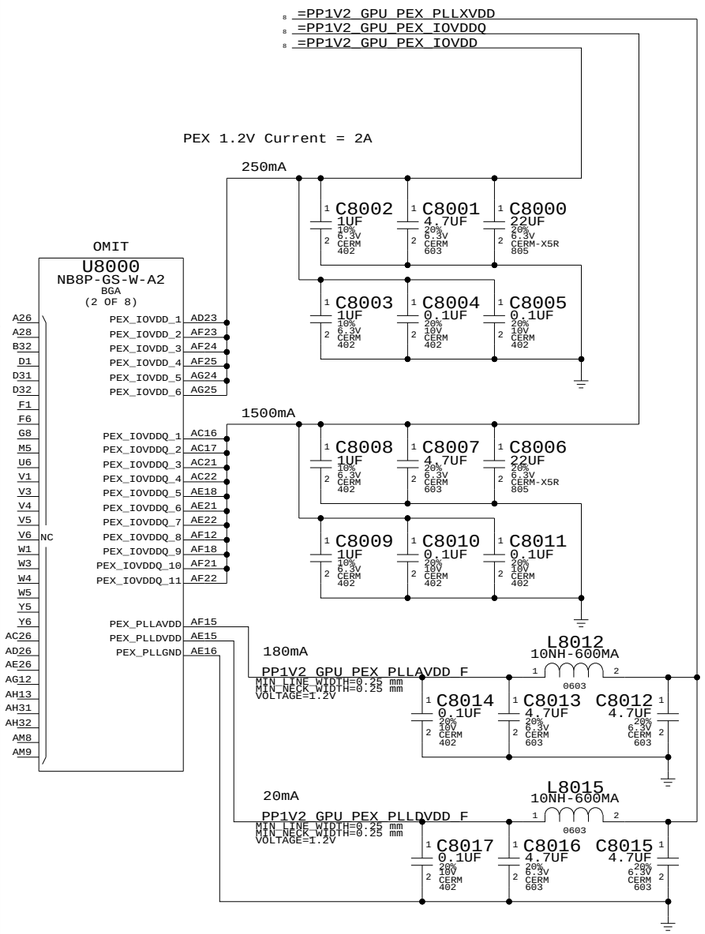
SCALE NONE — SHT 65 OF 88

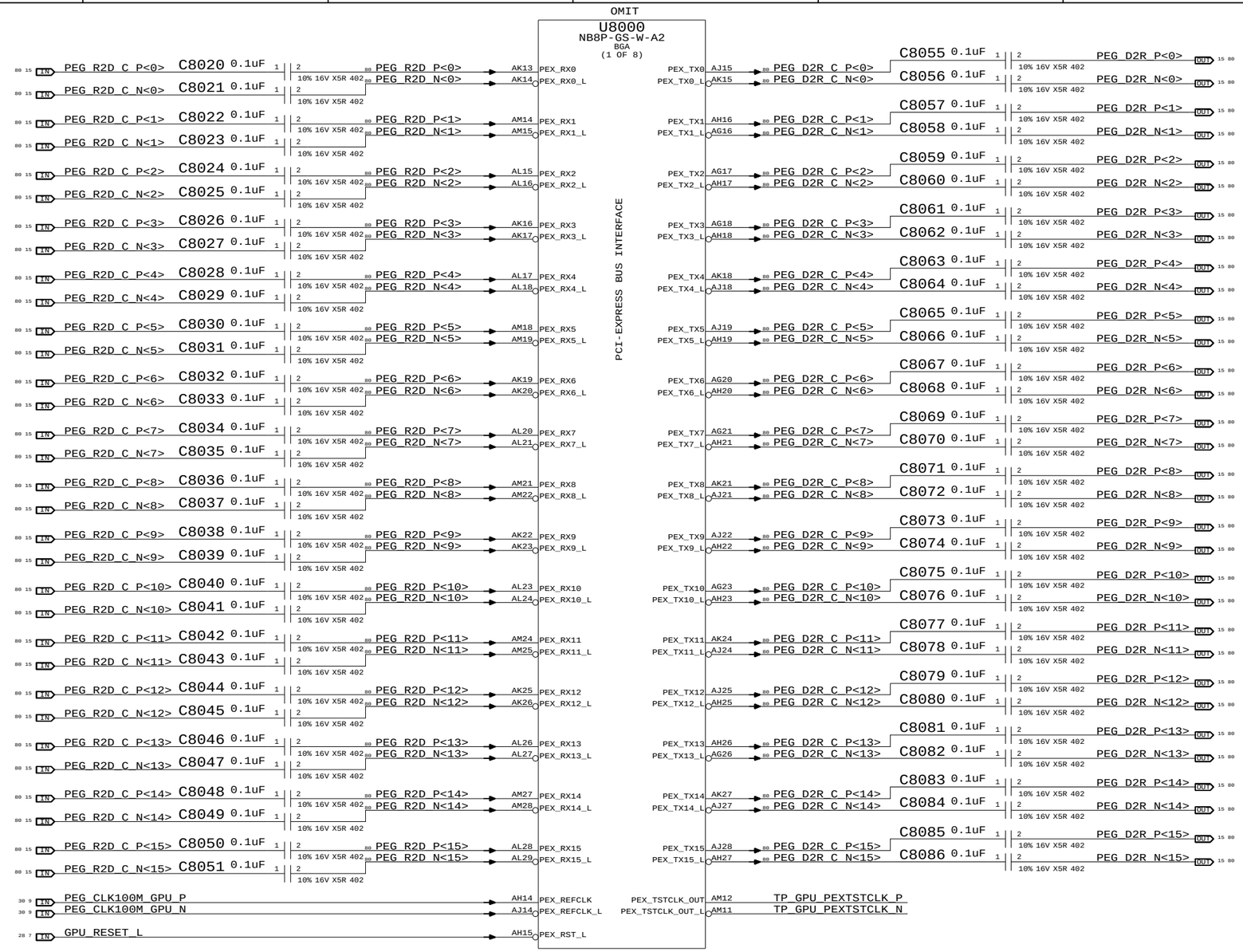
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

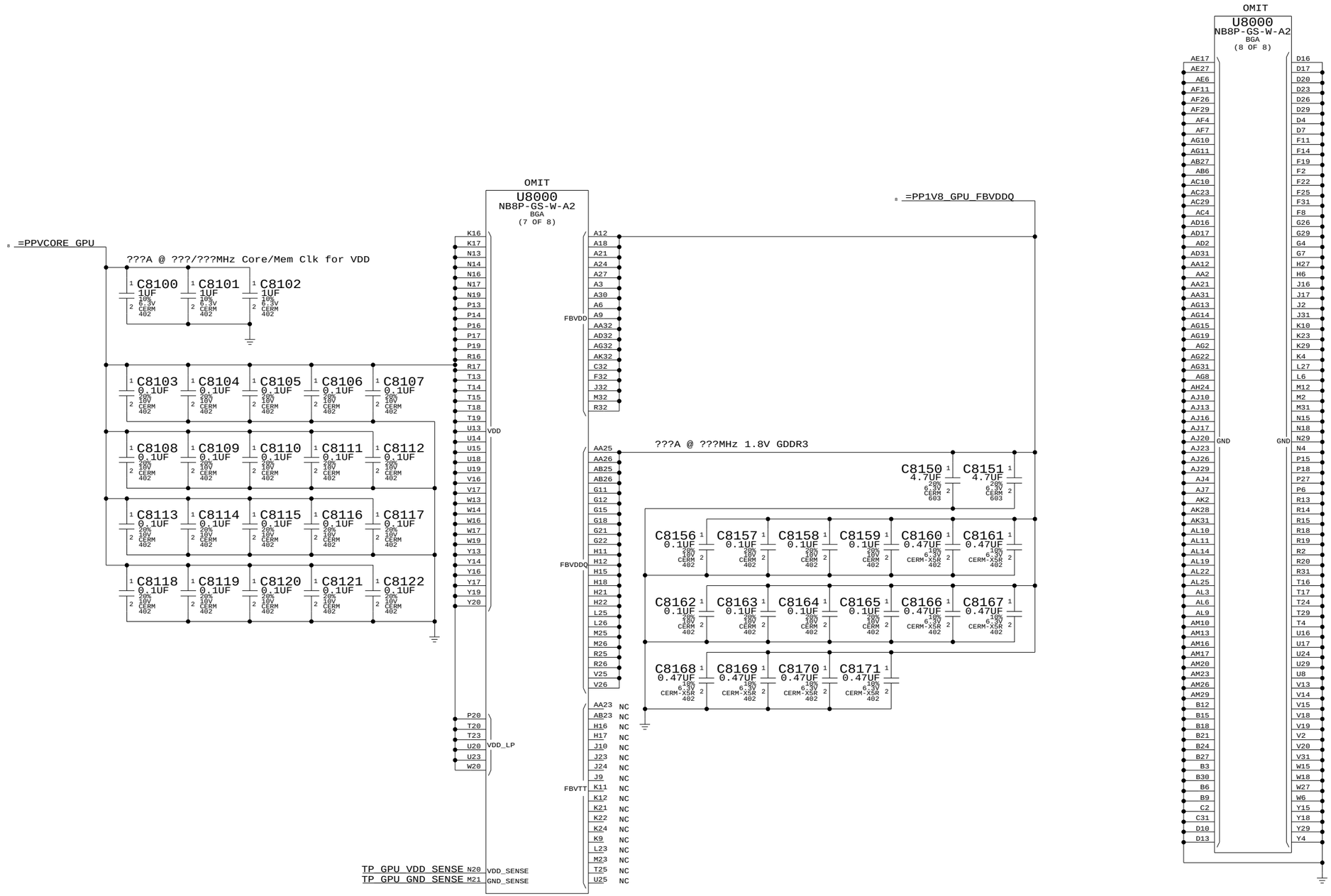
SCALE NONE | SHT 66 OF 88

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

SCALE NONE

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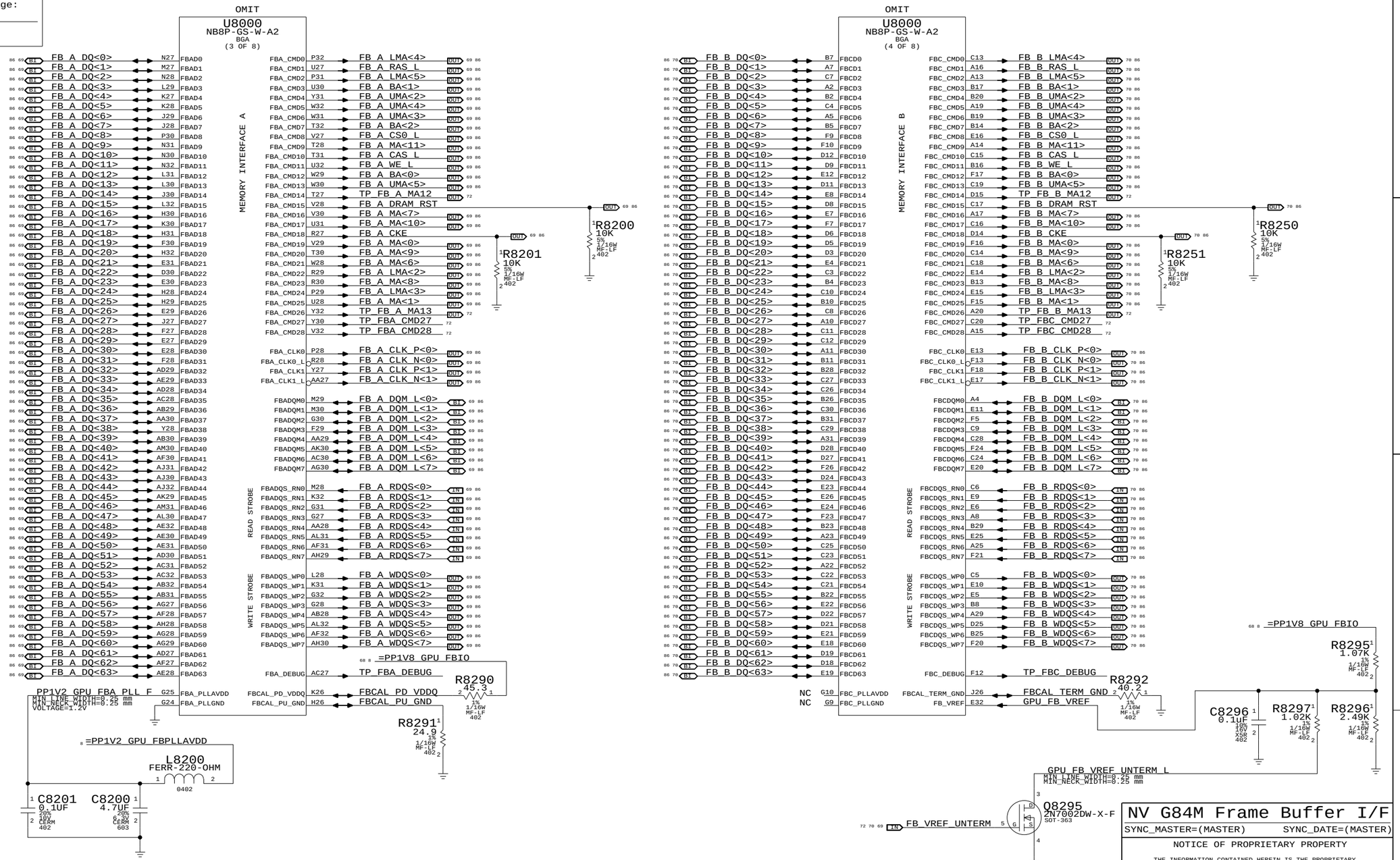
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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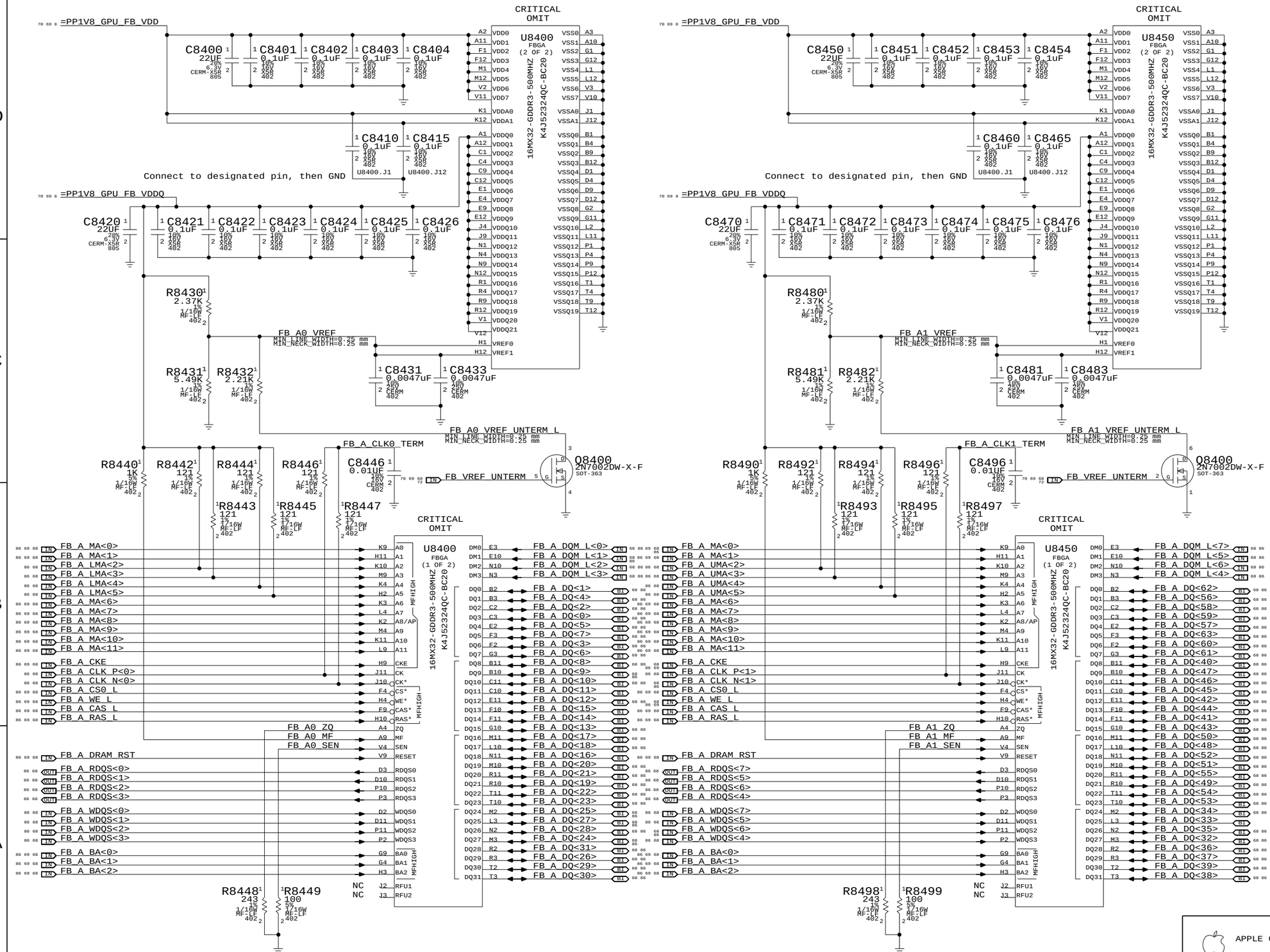
D	051-7225	A.0.0

SCALE NONE

SHT 68 OF 88



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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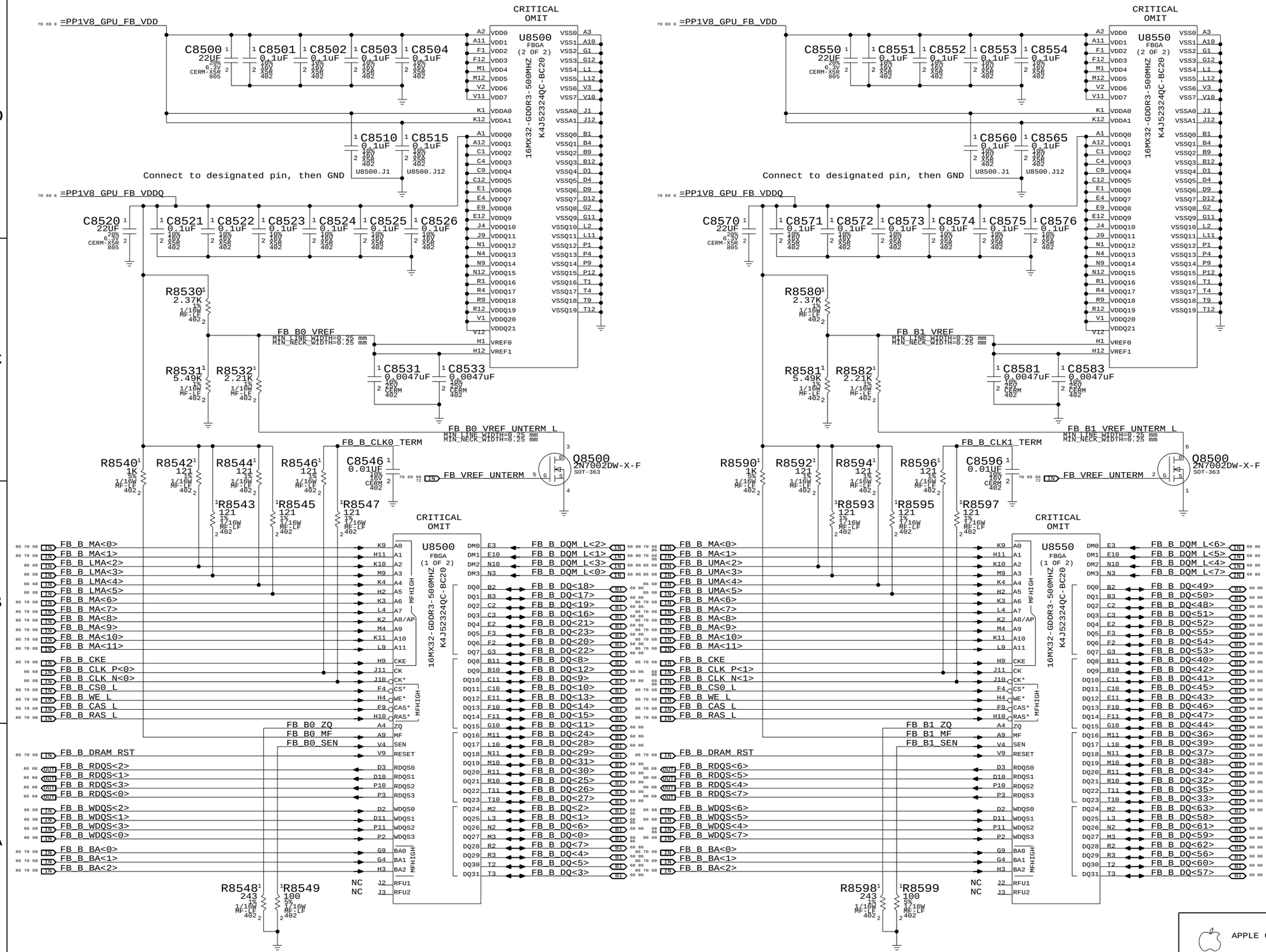
SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

SCALE NONE

SHT 69 OF 88



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

SCALE NONE

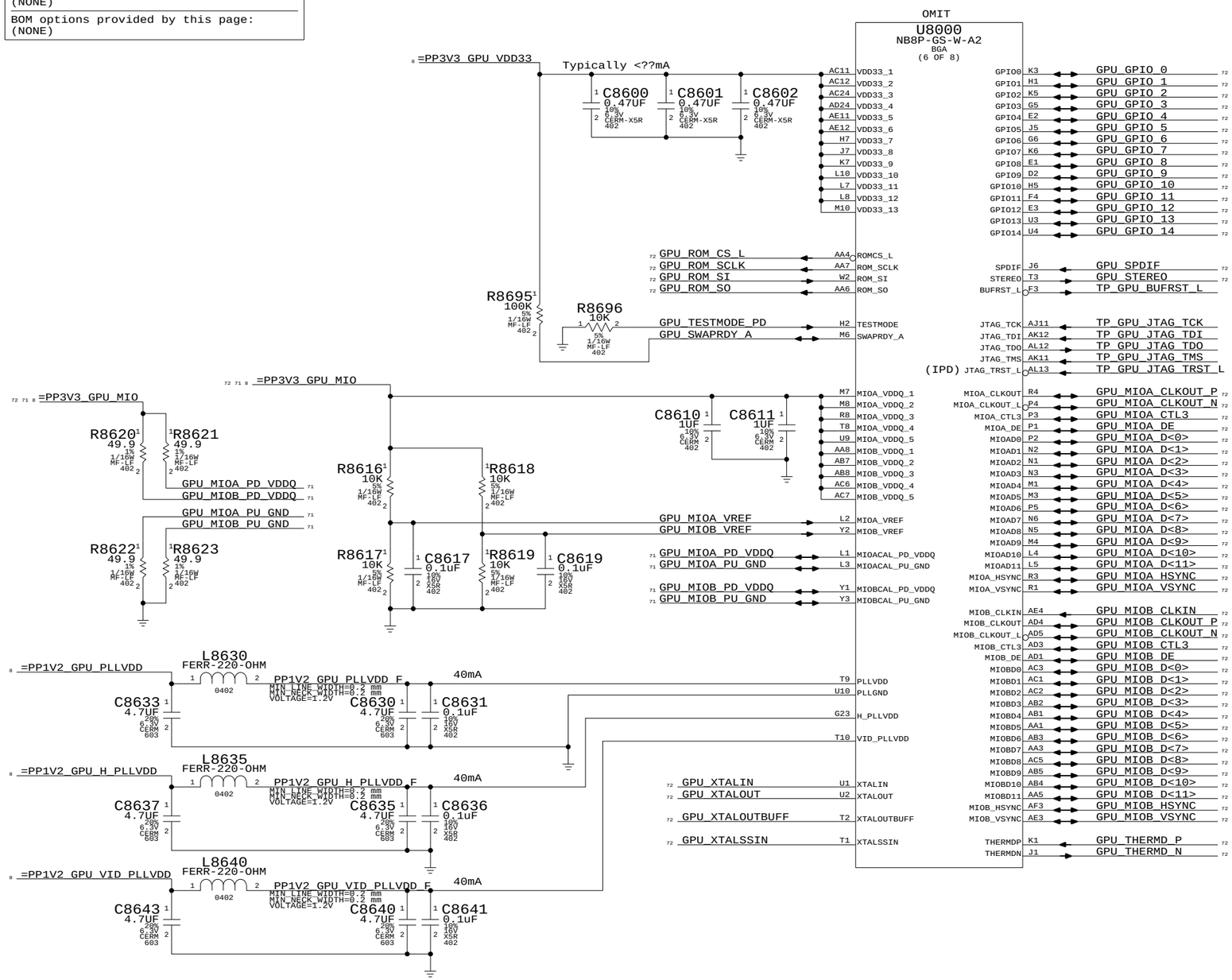
SHT 70 OF 88

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

SCALE NONE | SHT 71 OF 88

GPIOs

	Native Func		
GPU_GPIO_0	HPD0	GPU_HPD (MAKE_BASE=TRUE)	IN 76
GPU_GPIO_1	HPD1	NC_GPU_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=TRUE)	
GPU_GPIO_2	LCD0_BL_PWM	GPU_BL_PWM (MAKE_BASE=TRUE)	OUT 77
GPU_GPIO_3	LCD0_VDD	GPU_PANEL_EN (MAKE_BASE=TRUE)	OUT 77
GPU_GPIO_4	LCD0_BL_EN	GPU_BKLT_EN (MAKE_BASE=TRUE)	OUT 77
GPU_GPIO_5	VID0	GPU_VCORE_VID0 (MAKE_BASE=TRUE)	OUT 74
GPU_GPIO_6	VID1	GPU_VCORE_VID1 (MAKE_BASE=TRUE)	OUT 74
GPU_GPIO_7	MEM_VID	GPU_VGA_EN_L (MAKE_BASE=TRUE)	72
GPU_GPIO_8	THERM	NC_GPU_GPIO_8 (MAKE_BASE=TRUE, NO_TEST=TRUE)	
GPU_GPIO_9	FAN_PWM	TP_GPU_GSTATE<0> (MAKE_BASE=TRUE)	
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM (MAKE_BASE=TRUE)	OUT 68 69 70
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID2 (MAKE_BASE=TRUE)	OUT 74
GPU_GPIO_12	AC_DET	TP_GPU_GSTATE<1> (MAKE_BASE=TRUE)	
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_PWRCTL0 (MAKE_BASE=TRUE)	OUT 74
GPU_GPIO_14	PWR_CTL1	GPU_VCORE_PWRCTL1 (MAKE_BASE=TRUE)	OUT 74

Renamed signals

86 30 GPU_CLK27M_GATED (MAKE_BASE=TRUE)	GPU_XTALIN 71
86 30 GPU_CLK27M_SS_GATED (MAKE_BASE=TRUE)	GPU_XTALSSIN 71 72
87 51 GPU_TDIODE_P (MAKE_BASE=TRUE)	GPU_THERMD_P 71
51 GPU_TDIODE_N (MAKE_BASE=TRUE)	GPU_THERMD_N 71
76 GPU_DVI_DDC_CLK (MAKE_BASE=TRUE)	GPU_I2CB_SCL 73
76 GPU_DVI_DDC_DATA (MAKE_BASE=TRUE)	GPU_I2CB_SDA 73
77 GPU_PANEL_DDC_CLK (MAKE_BASE=TRUE)	GPU_I2CC_SCL 73
77 GPU_PANEL_DDC_DATA (MAKE_BASE=TRUE)	GPU_I2CC_SDA 73

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	GPU_XTALOUT 71
NC_GPU_SPDIF (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_SPDIF 71
NC_GPU_STEREO (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_STEREO 71
NC_FB_A_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FB_A_MA12 68
NC_FB_B_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FB_B_MA12 68
NC_FB_A_MA13 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FB_A_MA13 68
NC_FB_B_MA13 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FB_B_MA13 68
NC_FBA_CMD27 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FBA_CMD27 68
NC_FBC_CMD27 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FBC_CMD27 68
NC_FBA_CMD28 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FBA_CMD28 68
NC_FBC_CMD28 (MAKE_BASE=TRUE, NO_TEST=TRUE)	TP_FBC_CMD28 68
NC_GPU_ROM_CS_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_ROM_CS_L 71
NC_GPU_ROM_SCLK (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_ROM_SCLK 71
NC_GPU_ROM_SI (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_ROM_SI 71
NC_GPU_ROM_SO (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_ROM_SO 71
NC_GPU_CSYNC (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_CSYNC 73
NC_GPU_R2 (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_R2 73
NC_GPU_G2 (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_G2 73
NC_GPU_B2 (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_B2 73
NC_GPU_H2SYNC (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_H2SYNC 73
NC_GPU_V2SYNC (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_V2SYNC 73
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_U_DATA_P<3> 73 86
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_U_DATA_N<3> 73 86
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_L_DATA_P<3> 73 86
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_L_DATA_N<3> 73 86
TP_GPU_MIOA_CLKOUT_P (MAKE_BASE=TRUE)	GPU_MIOA_CLKOUT_P 71
TP_GPU_MIOA_CLKOUT_N (MAKE_BASE=TRUE)	GPU_MIOA_CLKOUT_N 71
TP_GPU_MIOA_CTL3 (MAKE_BASE=TRUE)	GPU_MIOA_CTL3 71
TP_GPU_MIOA_DE (MAKE_BASE=TRUE)	GPU_MIOA_DE 71
TP_GPU_MIOA_D<5..2> (MAKE_BASE=TRUE)	GPU_MIOA_D<5..2> 71
TP_GPU_MIOA_D<7> (MAKE_BASE=TRUE)	GPU_MIOA_D<7> 71
TP_GPU_MIOA_D<11..10> (MAKE_BASE=TRUE)	GPU_MIOA_D<11..10> 71
TP_GPU_MIOA_HSYNC (MAKE_BASE=TRUE)	GPU_MIOA_HSYNC 71
TP_GPU_MIOA_VSYNC (MAKE_BASE=TRUE)	GPU_MIOA_VSYNC 71
TP_GPU_MIOB_CLKIN (MAKE_BASE=TRUE)	GPU_MIOB_CLKIN 71
TP_GPU_MIOB_CLKOUT_P (MAKE_BASE=TRUE)	GPU_MIOB_CLKOUT_P 71
TP_GPU_MIOB_CLKOUT_N (MAKE_BASE=TRUE)	GPU_MIOB_CLKOUT_N 71
TP_GPU_MIOB_DE (MAKE_BASE=TRUE)	GPU_MIOB_DE 71
TP_GPU_MIOB_CTL3 (MAKE_BASE=TRUE)	GPU_MIOB_CTL3 71
TP_GPU_MIOB_D<2> (MAKE_BASE=TRUE)	GPU_MIOB_D<2> 71
TP_GPU_MIOB_D<7..6> (MAKE_BASE=TRUE)	GPU_MIOB_D<7..6> 71
TP_GPU_MIOB_D<11..10> (MAKE_BASE=TRUE)	GPU_MIOB_D<11..10> 71
TP_GPU_MIOB_VSYNC (MAKE_BASE=TRUE)	GPU_MIOB_VSYNC 71
NC_GPU_IFPD_CLK_P (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_IFPD_CLK_P 73
NC_GPU_IFPD_CLK_N (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_IFPD_CLK_N 73

Unused I2C Buses

NC_GPU_I2CA_SCL (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_I2CA_SCL 73
NC_GPU_I2CA_SDA (MAKE_BASE=TRUE, NO_TEST=TRUE)	GPU_I2CA_SDA 73

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Config Straps

=PP3V3_GPU_MIO (72 71 8)

Supported straps:									
	VRAM_SAMSUNG		VRAM_128	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
	R8720[1] 10K	R8722[1] 10K	R8724[1] 10K	R8726[1] 10K	R8728[1] 1K	R8729[1] 1K	R8730[1] 1K	R8731[1] 1K	R8732[1] 1K
RAMCFG0	GPU_MIOB_D<0>								
RAMCFG1		GPU_MIOB_D<1>							
RAMCFG2			GPU_MIOB_D<8>						
RAMCFG3				GPU_MIOB_D<9>					
3GIO_PADCFG0					GPU_MIOA_D<6>				
3GIO_PADCFG1						GPU_MIOA_D<8>			
3GIO_PADCFG2							GPU_MIOA_D<9>		
3GIO_PADCFG3								GPU_MIOB_HSYNC	
PEX_PLL_EN_TERM									GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)									GPU_MIOA_D<1>
PCI_DEVID<2..0>	VRAM_HYNIX R8721[1] 10K	NO STUFF R8723[1] 10K	VRAM_256 R8725[1] 10K	R8727[1] 10K					R8733[1] 1K

=PP3V3_GPU_MIO (72 71 8)

Straps not supported:	
USER<3..0>	MIOA_D<5..2>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
PCI_DEVID<4..3>	MIOB_CTL3, MIOB_D<11>

R8735[1] 1K	R8736[1] 1K	R8737[1] 1K
PCI_DEVID2	GPU_MIOB_D<3>	
PCI_DEVID1	GPU_MIOB_D<5>	
PCI_DEVID0	GPU_MIOB_D<4>	

HDCP Support

=PP3V3_GPU_HDCP (8)

HDCP C8770 0.1UF (20% 16V CERM 402)

HDCP R8770[1] 10K 5% 1/16W MF-LF 402

HDCP CRITICAL U8770 AT88SC080C SOI

GPU_I2CH_SCL (73 BI) — SCL
GPU_I2CH_SDA (73 BI) — SDA

HDCP R8771[1] 10K 5% 1/16W MF-LF 402 — NC

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

=PP3V3_GPU_TMDS (8) — =PP3V3_GPU_TMDS_FET (8)

[1]R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

=GPUVCORE_EN (74 65 IN)

Q8925 2N7002DW-X-F SOT-363

R8791[1] 100K 5% 1/16W MF-LF 402

Unused Clocks

GPU_XTALSSIN (72 71)
GPU_XTALOUTBUFF (71)

GPU_SS_INT

R8780[1] 10K 5% 1/16W MF-LF 402

R8781[1] 10K 5% 1/16W MF-LF 402

Analog Video Mux

=PP3V3_GPU_VIDEOMUX (8)

C8700 0.1UF (20% 16V CERM 402)

CRITICAL OMIT

U8700 QFN TS3V330 (VCC 16)

GPU_VGA_R (86 73 IN)	S1A 2	DA 4	GPU_TV_C_VGA_R (OUT 76 86)
GPU_VGA_G (86 73 IN)	S2A 3		
GPU_VGA_B (86 73 IN)	S1B 5	DB 7	GPU_TV_Y_VGA_G (OUT 76 86)
	S2B 6		
	S1C 11	DC 9	GPU_TV_COMP_VGA_B (OUT 76 86)
	S2C 10		
	S1D 14	DD 12	NC
	S2D 13	IN 1	GPU_VGA_EN_L (72)
	THRML PAD 17	EN_L 15	
	GND 8		

Place Rs near GPU: R8740[1] 150 1% 1/16W MF-LF 402; R8741[1] 150 1% 1/16W MF-LF 402; R8742[1] 150 1% 1/16W MF-LF 402

GPU_TV_C (86 73 IN)
GPU_TV_Y (86 73 IN)
GPU_TV_COMP (86 73 IN)

Place Rs near GPU: R8743[1] 150 1% 1/16W MF-LF 402; R8744[1] 150 1% 1/16W MF-LF 402; R8745[1] 150 1% 1/16W MF-LF 402

[1]R8700 10K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1718	1	IC,TS3V340,QUAD VIDEO SW,QFN16	U8700	CRITICAL	

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1579	353S1718		ALL (U8700)	TS3V330 alt to TS3V340

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7225	A.0.0

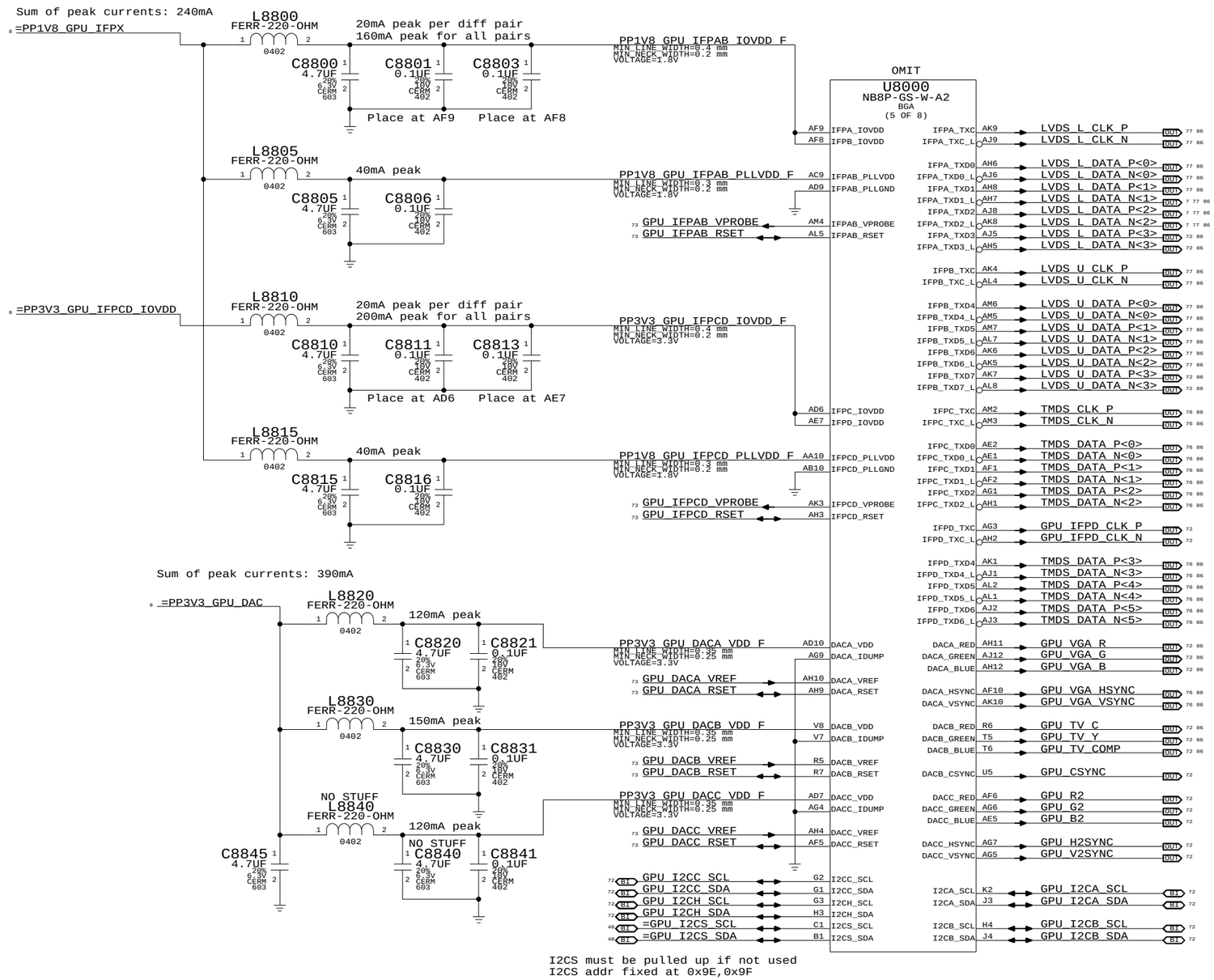
SCALE NONE — SHT 72 OF 88

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

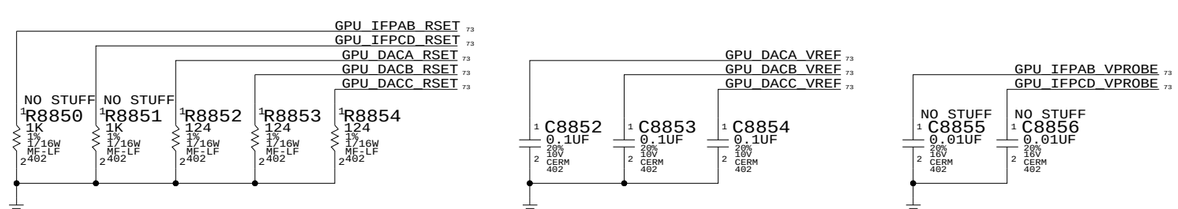
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb



NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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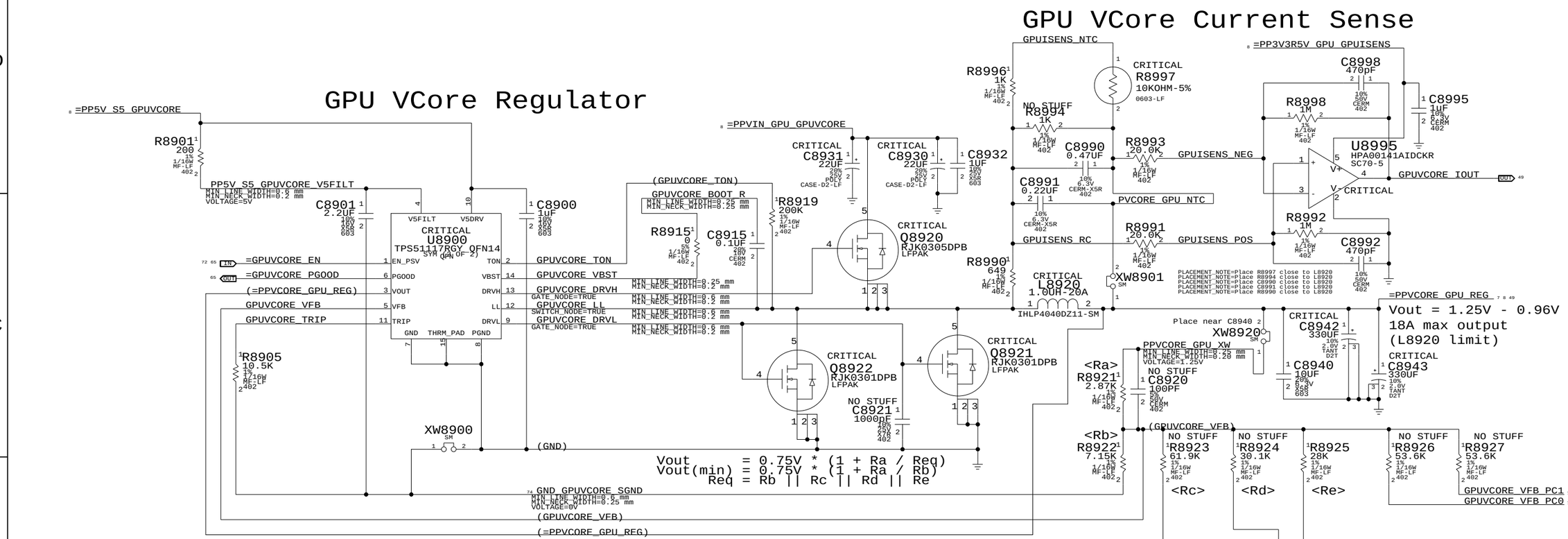

GPU VCore Setpoints

VID2	VID1	VID0	C D E	State
0	0	0	- - -	1.050V (rsvd state)
0	0	1	Y - -	1.050V (max batt)
0	1	1	Y Y -	1.050V (balanced)
1	1	1	Y Y Y	1.125V (max perf)

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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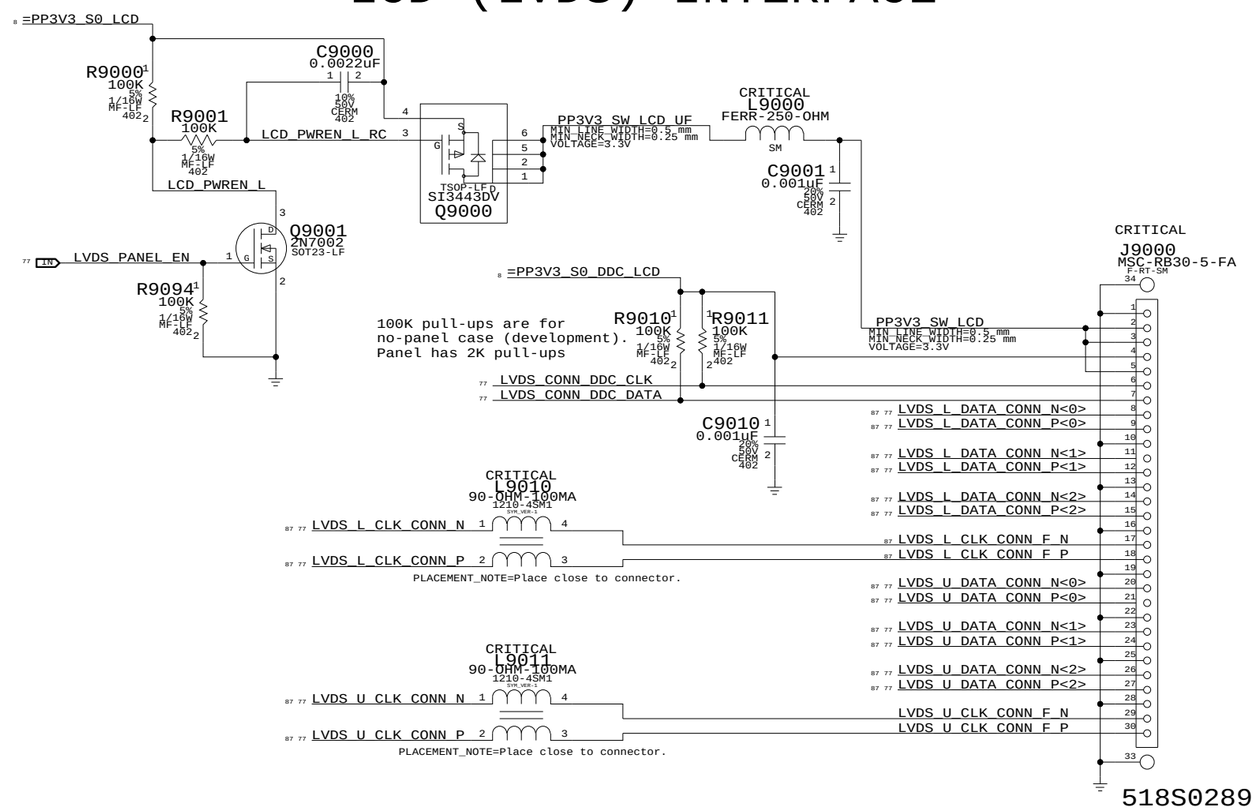
SCALE: NONE SHT 74 OF 88

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS DATA N<0> — NO STUFF R9462 49.9 1% 1/16W MF-LF 402 — CRITICAL L9460 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<0>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9462 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R0 — NO STUFF R9463 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<0>
TMDS DATA P<0> — PLACEMENT_NOTE=Place close to connector.

TMDS DATA N<1> — NO STUFF R9466 49.9 1% 1/16W MF-LF 402 — CRITICAL L9464 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<1>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9466 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R1 — NO STUFF R9467 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<1>
TMDS DATA P<1> — PLACEMENT_NOTE=Place close to connector.

TMDS DATA N<2> — NO STUFF R9470 49.9 1% 1/16W MF-LF 402 — CRITICAL L9468 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<2>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9470 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R2 — NO STUFF R9471 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<2>
TMDS DATA P<2> — PLACEMENT_NOTE=Place close to connector.

TMDS CLK N — R9472 0 5% 1/16W MF-LF 402 — TMDS CLK R N — CRITICAL L9472 370-OHM SM — TMDS CLK F N
=PP3V3_GPU_TMDSBIAS — NO STUFF R9474 49.9 1% 1/16W MF-LF 402 — NO STUFF C9474 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS CLK CMF — NO STUFF R9475 49.9 1% 1/16W MF-LF 402 — TMDS CLK F P
PLACEMENT_NOTE=Place close to connector.
TMDS CLK P — R9473 0 5% 1/16W MF-LF 402 — TMDS CLK R P

TMDS DATA N<3> — NO STUFF R9478 49.9 1% 1/16W MF-LF 402 — CRITICAL L9476 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<3>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9478 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R3 — NO STUFF R9479 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<3>
TMDS DATA P<3> — PLACEMENT_NOTE=Place close to connector.

TMDS DATA N<4> — NO STUFF R9482 49.9 1% 1/16W MF-LF 402 — CRITICAL L9480 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<4>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9482 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R4 — NO STUFF R9483 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<4>
TMDS DATA P<4> — PLACEMENT_NOTE=Place close to connector.

TMDS DATA N<5> — NO STUFF R9486 49.9 1% 1/16W MF-LF 402 — CRITICAL L9484 90-OHM-100MA 1210-4SM1 — TMDS DATA F N<5>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9486 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS DATA R5 — NO STUFF R9487 49.9 1% 1/16W MF-LF 402 — TMDS DATA F P<5>
TMDS DATA P<5> — PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC — U9450 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector. — R9450 33 5% 1/16W MF-LF 402
GPU_VGA_VSYNC — C9450 0.1uF 20% 16V CERM 402 — VGA_VSYNC_R — VGA_VSYNC

=PP3V3_GPU_VGASYNC — U9451 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector. — R9451 33 5% 1/16W MF-LF 402
GPU_VGA_HSYNC — C9451 0.1uF 20% 16V CERM 402 — VGA_HSYNC_R — VGA_HSYNC

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B — VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 — VGA_B (DACB TV COMP) — C9440 3.3pF 0.25% 50V CERM 402
GPU_TV_Y_VGA_G — VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 — VGA_G (DACB TV Y) — C9441 3.3pF 0.25% 50V CERM 402
GPU_TV_C_VGA_R — VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 — VGA_R (DACB TV C) — C9442 3.3pF 0.25% 50V CERM 402

CRITICAL FL9440 210MHZ MEA2010P-SM

DVI INTERFACE

DVI DDC Current Limit

(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC — CRITICAL F9410 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_F (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — CRITICAL L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)

Isolation required for DVI->ADC Adapter

D9410 SOD-123 — PP5V_S0_DDC_PULLUPS (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — B0530WXF

=GND_CHASSIS_DVI_BOT — CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
TMDS_DATA_F_P<0>	18	9	TMDS_DATA_F_N<1>
	19	2	TMDS_DATA_F_P<2>
		10	TMDS_DATA_F_P<1>
		3	
TMDS_DATA_F_N<5>	20	11	
TMDS_DATA_F_P<5>	21	4	TMDS_DATA_F_N<4>
		12	TMDS_DATA_F_N<3>
		5	TMDS_DATA_F_P<4>
		13	TMDS_DATA_F_P<3>
	22	6	DVI_DDC_CLK_R
		14	(PP5V_S0_DDC)
TMDS_CLK_F_P	23	7	DVI_DDC_DATA_R
		15	
TMDS_CLK_F_N	24	8	VGA_VSYNC
		16	DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	34	32	

514-0278

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402 — VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402 — VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402 — C9410 0.01UF 5% 50V CERM 603

C9411 100pF 5% 50V CERM 402 — C9413 100pF 5% 50V CERM 402 — C9414 100pF 5% 50V CERM 402

=GND_CHASSIS_DVI_TOP — OMIT CX9490 SHORT NONE NONE 402 — OMIT CX9491 SHORT NONE NONE 402 — OMIT CX9492 SHORT NONE NONE 402 — OMIT CX9493 SHORT NONE NONE 402
=GND_CHASSIS_DVI_BOT — OMIT CX9400 SHORT NONE NONE 402 — OMIT CX9401 SHORT NONE NONE 402 — OMIT CX9402 SHORT NONE NONE 402 — OMIT CX9403 SHORT NONE NONE 402

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI

R9410 4.7K 5% 1/16W MF-LF 402 — R9412 4.7K 5% 1/16W MF-LF 402 — R9411 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK — Q9411 2N7002DW-X-F SOT-363 — R9420 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK (OUT)
R9413 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA — Q9411 2N7002DW-X-F SOT-363 — R9421 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA (OUT)
GPU_HPD_BILAT — =GPU_HPD_ENABLE (IN) — Q9414 2N7002DW-X-F SOT-363 — R9422 270K 5% 1/16W MF-LF 402
R9414 100 5% 1/16W MF-LF 402 — DVI_HPD — GPU_HPD (OUT)
=PP5V_S0_SB_HPD — Q9415 2N7002DW-X-F SOT-363 — R9423 270K 5% 1/16W MF-LF 402 — DVI_HOTPLUG_DET (OUT)
R9415 20K 5% 1/16W MF-LF 402

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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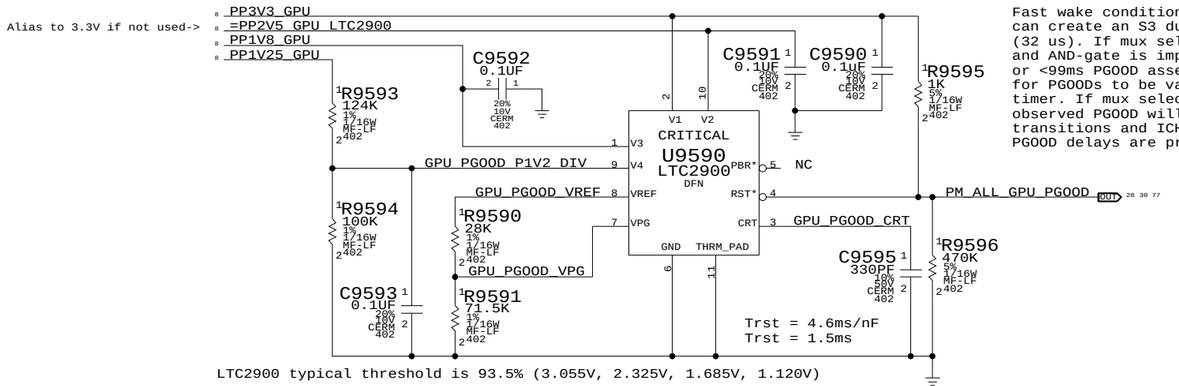
PGOOD Monitor for GPU Rails

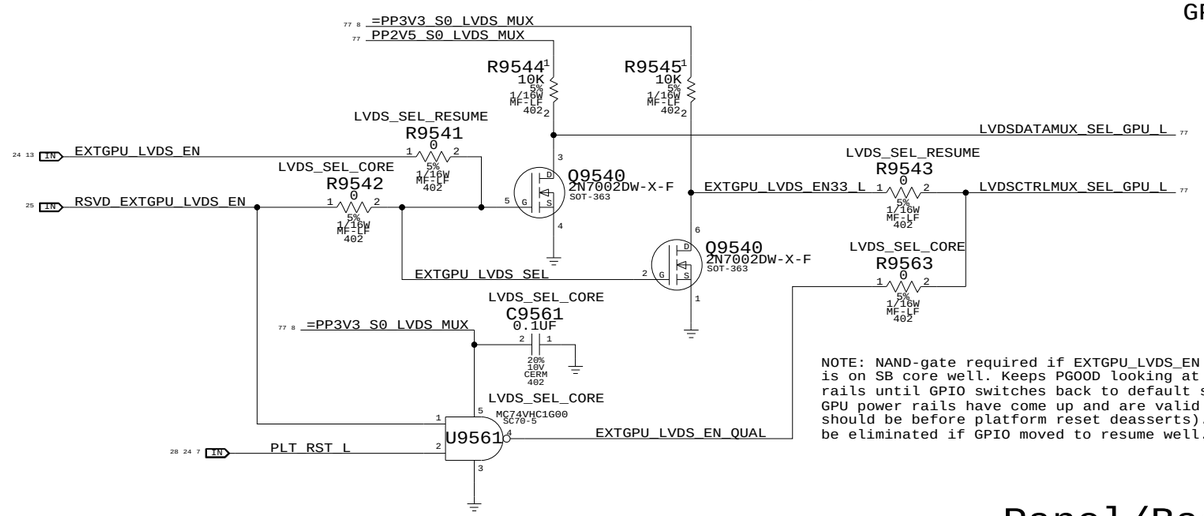
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

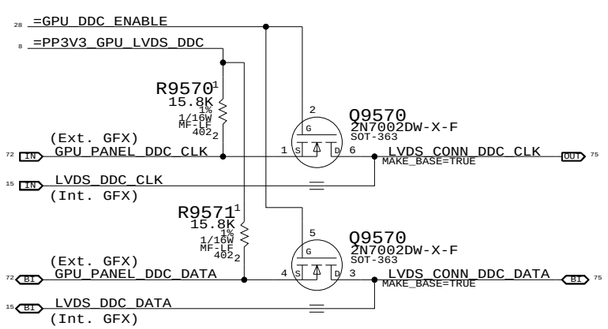
Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

Mux Select Conditioning

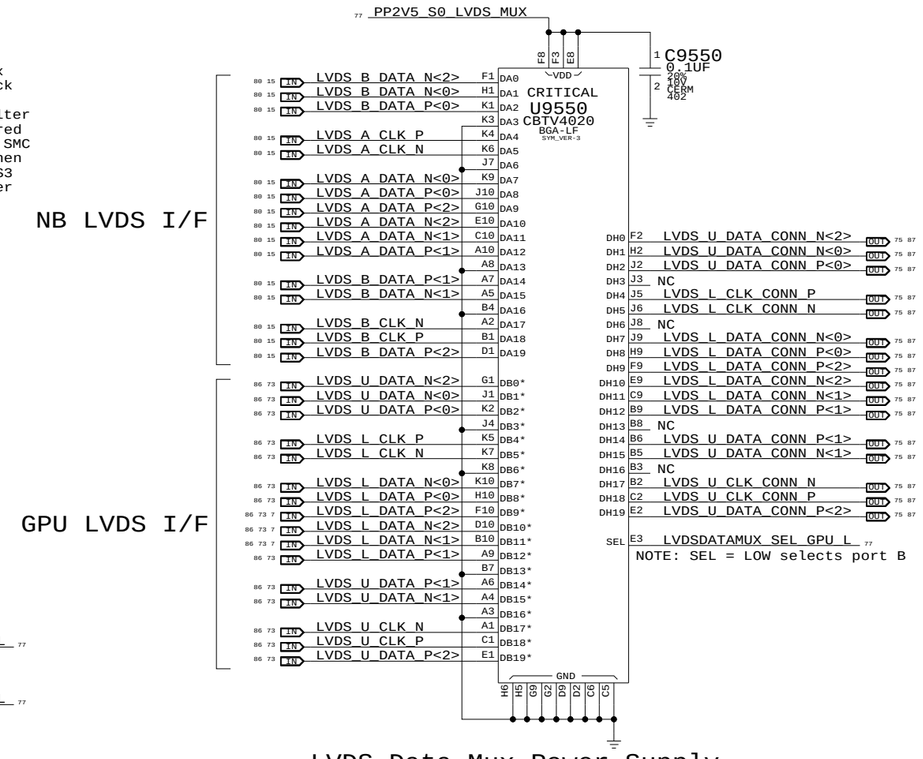


NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

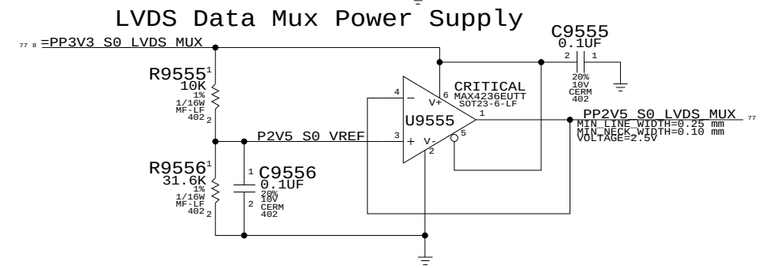
GPU DDC Pass FETs



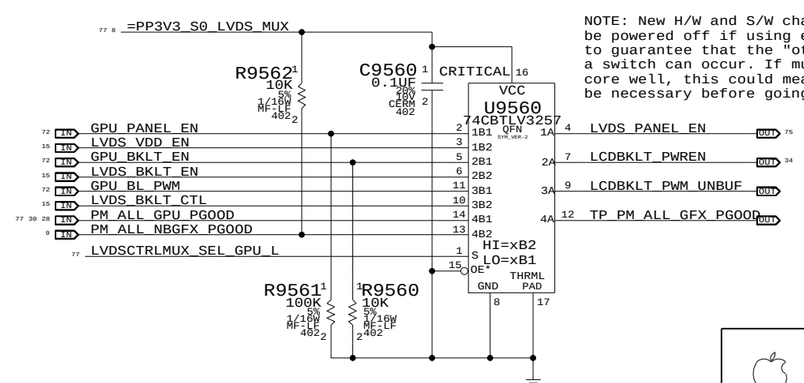
LVDS I/F Mux



LVDS Data Mux Power Supply



Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

LVDS Interface Mux

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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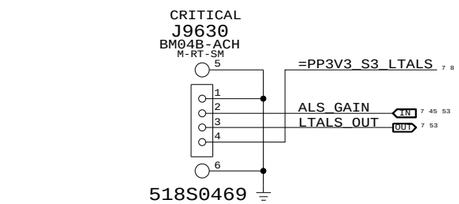
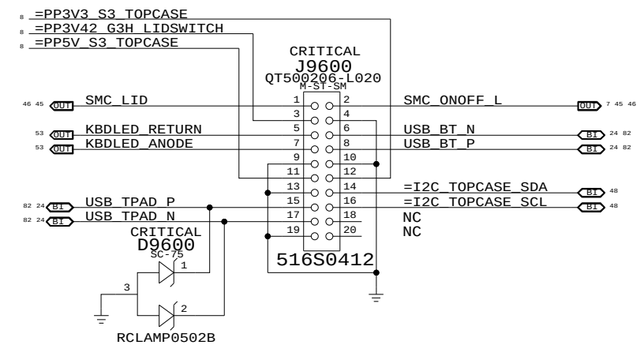
Left ALS Connector

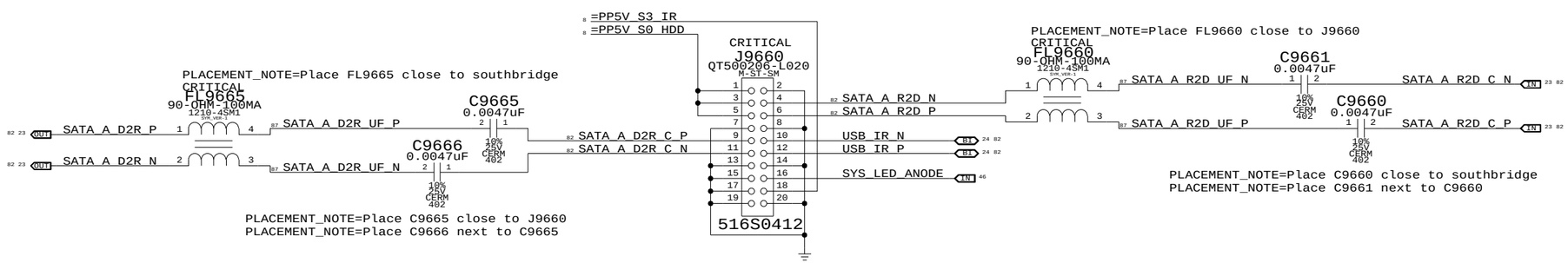


White colored version of 518S0369

Top-Case Connector



SATA HDD & IR & SIL Flex Connector



NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 58
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 84
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

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D	051-7225	A.0.0

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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 66
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	66
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	66
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

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D	051-7225	A.0.0

SCALE NONE SHT 80 OF 88

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0

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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 78
	SATA_100D	SATA	SATA_A_R2D_C_N	23 78
	SATA_100D	SATA	SATA_A_R2D_P	78
	SATA_100D	SATA	SATA_A_R2D_N	78
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 78
	SATA_100D	SATA	SATA_A_D2R_N	23 78
	SATA_100D	SATA	SATA_A_D2R_C_P	78
	SATA_100D	SATA	SATA_A_D2R_C_N	78
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	24 44
	USB_90D	USB	USB_EXTD_N	24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 44
	USB_90D	USB	USB_CAMERA_N	7 24 44
USB_BT	USB_90D	USB	USB_BT_P	24 78
	USB_90D	USB	USB_BT_N	24 78
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 78
	USB_90D	USB	USB_TPAD_N	24 78
USB_IR	USB_90D	USB	USB_IR_P	24 78
	USB_90D	USB	USB_IR_N	24 78
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 24
	USB_90D	USB	USB_EXTC_N	9 24
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 55
	SPI_55S	SPI	SPI_SCLK	55
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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D	051-7225	A.0.0

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1 L	24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1 L	
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2 L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2 L	
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIRQC L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIRQD L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT PIRQE L	24
INT_PIRQF_L	PCI_55S	PCI	INT PIRQF L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	
	PCIE_100D	PCIE	PCIE A R2D C N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	
	PCIE_100D	PCIE	PCIE A D2R N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	
	PCIE_100D	PCIE	PCIE B R2D C N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	
	PCIE_100D	PCIE	PCIE B D2R N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	34
	PCIE_100D	PCIE	PCIE EXCARD R2D C N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	34
	PCIE_100D	PCIE	PCIE EXCARD D2R N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	
	PCIE_100D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	
	PCIE_100D	PCIE	PCIE FW D2R N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
	PCIE_100D	PCIE	PCIE ENET R2D P	35
	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
	PCIE_100D	PCIE	PCIE ENET D2R C P	35
	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

SB Constraints (2 of 2)

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SCALE NONE	SHT 83 OF 88	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 79
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 79
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 22 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 22 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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D	051-7225	A.0.0

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41
Port 2 Not Used				

FireWire Constraints

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D	051-7225	A.0.0

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	68 69
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	68 69
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	68 69
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<1..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<11..6>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_BA<2..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_RAS_L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CAS_L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_WE_L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CKE	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CS0_L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_DRAM_RST	68 69
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2>	68 69
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2>	68 69
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0>	68 69
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1>	68 69
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2>	68 69
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3>	68 69
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0>	68 69
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1>	68 69
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2>	68 69
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3>	68 69
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0>	68 69
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8>	68 69
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16>	68 69
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24>	68 69
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0>	68 69
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1>	68 69
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2>	68 69
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3>	68 69
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4>	68 69
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5>	68 69
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6>	68 69
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7>	68 69
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4>	68 69
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5>	68 69
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6>	68 69
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7>	68 69
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32>	68 69
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40>	68 69
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48>	68 69
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56>	68 69
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4>	68 69
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5>	68 69
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6>	68 69
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7>	68 69

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED	30 72
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED	30 72
	LVDS_100D	LVDS	LVDS_L_CLK_P	73 77
	LVDS_100D	LVDS	LVDS_L_CLK_N	73 77
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	7 72 73 77
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	7 72 73 77
	LVDS_100D	LVDS	LVDS_U_CLK_P	73 77
	LVDS_100D	LVDS	LVDS_U_CLK_N	73 77
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	72 73 77
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	72 73 77
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	73 76
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>	73 76
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	72 76
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	72 76
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	72 76
	VGA_50S	VGA	GPU_VGA_R	72 73
	VGA_50S	VGA	GPU_VGA_G	72 73
	VGA_50S	VGA	GPU_VGA_B	72 73
	VGA_50S	VGA	GPU_TV_C	72 73
	VGA_50S	VGA	GPU_TV_Y	72 73
	VGA_50S	VGA	GPU_TV_COMP	72 73
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	73 76
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	73 76

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	68 70
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	68 70
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	68 70
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<1..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<11..6>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_BA<2..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_RAS_L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CAS_L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_WE_L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CKE	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CS0_L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_DRAM_RST	68 70
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2>	68 70
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2>	68 70
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0>	68 70
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1>	68 70
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2>	68 70
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3>	68 70
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0>	68 70
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1>	68 70
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2>	68 70
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3>	68 70
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0>	68 70
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8>	68 70
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16>	68 70
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24>	68 70
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0>	68 70
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1>	68 70
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2>	68 70
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3>	68 70
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4>	68 70
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5>	68 70
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6>	68 70
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7>	68 70
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4>	68 70
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5>	68 70
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6>	68 70
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7>	68 70
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32>	68 70
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40>	68 70
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48>	68 70
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56>	68 70
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4>	68 70
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5>	68 70
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6>	68 70
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7>	68 70

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA

SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

M75 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	78
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	78
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	44
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	59
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 72
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	REMTHMSNS_DX_P	
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0>	75 77
	TMDS_100D	TMDS	TMDS_CLK_R_P	76
	TMDS_100D	TMDS	TMDS_CLK_R_N	76
	TMDS_100D	TMDS	TMDS_CLK_F_P	76
	TMDS_100D	TMDS	TMDS_CLK_F_N	76
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	76
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	76
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	76
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	76
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	76
		PP1V8_MEM	=PP1V8_S3M_MEM_A	8 31
		PP1V8_MEM	=PP1V8_S3M_MEM_B	8 32
		GND	GND	
		SB_POWER	PP3V3_S5	8
		SB_POWER	PP3V3_S0	8 65
		SB_POWER	PP1V5_S0	8
	WWAN_SIM	WWAN_SIM	WWAN_SIM_CLOCK	44
	WWAN_SIM	WWAN_SIM	WWAN_SIM_DATA	44

Project Specific Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7225	A.0.0
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M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

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